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OPEN AND DISTANCE LEARNING (ODL) PROGRAMMES

(FOR THOSE WHO JOINED THE PROGRAMMES FROM THE ACADEMIC YEAR 2023–2024)

I M.Sc. Physics

LINEAR AND DIGITAL ICs AND APPLICATIONS

Course Material

Prepared

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Tirunelveli - 12

LINEAR AND DIGITAL ICs AND APPLICATIONS

UNIT I:

INTEGRATED CIRCUITS AND OPERATION AMPLIFIER

Introduction, Classification of IC's, basic information of Op-Amp 741 and its features, the ideal Operational amplifier, Op-Amp internal circuit diagram, Op-Amp. Characteristics, DC and AC performance Characteristics

UNIT II:

APPLICATIONS OF OP-AMP

LINEAR APPLICATIONS OF OP-AMP: Solution to simultaneous equations and differential equations, Instrumentation amplifiers, V to I and I to V converters

NON - LINEAR APPLICATIONS OF OP-AMP: Sample and Hold circuit ,Log and Antilog amplifier, multiplier and divider Comparators, Schmit trigger, Multivibrators, Triangular and Square waveform generators

UNIT III

ACTIVE FILTERS & TIMERAND PHASE LOCKED LOOPS

ACTIVEFILTERS: Introduction, Butter worth filters–1st order,2nd order low and high pass filters, band pass, band reject and all pass filters.

TIMER AND PHASE LOCKED LOOPS :Introduction to IC 555timer description of functional diagram, mono stable and astable operations and applications, Schmitt trigger, PLL-introduction, basic principle, phase detector /comparator, voltage controlled oscillator (IC566), low pass filter monolithic PLL and applications of PLL

UNIT IV:

VOLTAGE REGULATOR & D to A AND A to D CONVERTERS

VOLTAG EREGULATOR: Introduction, Series Op-Amp regulator, IC Voltage Regulators, IC 723 general purpose regulators, Switching Regulator.

D to A AND A to D CONVERTERS : Introduction, basic DAC techniques – weighted resistor DAC, R-2R ladder DAC ,inverted R-2R DAC, A to D converters-parallel comparator type ADC, counter type ADC ,successive approximation ADC and dual slope ADC, DAC and ADC Specification

UNIT V:

CMOS LOGIC, COMBINATIONAL CIRCUITS USING TTL 74XX ICs & SEQUENTIAL CIRCUITS USING TTL 74XX ICs

CMOS LOGIC : CMOS logic levels, MOS transistors, Basic CMOS Inverter, NAND and NOR gates, CMOS AND – OR – INVERT and OR- AND - INVERT gates, implementation of any function using CMOS logic.

COMBINATIONAL CIRCUITS USING TTL 74XX ICs: Study of logic gates using 74XX ICs, Four-bit parallel adder (IC7483),Comparator (IC 7485), Decoder (IC 74138, IC 74154), BCD to 7-segment decoder (IC7447), Encoder (IC74147), Multiplexer(IC74151), Demultiplexer (IC74154).

SEQUENTIAL CIRCUITS USING TTL 74XX ICs: Flip Flops (IC7474, IC7473), Shift Registers,Universal Shift Register (IC74194),4-bit asynchronous binary counter (IC7493).

UNIT I

INTEGRATED CIRCUITS AND OPERATIONAL AMPLIFIER

Introduction, Classification of IC's, basic information of Op-Amp 741 and its features, the ideal Operational amplifier, Op-Amp internal circuit and Op-Amp. Characteristics

1.1 Introduction

The integrated circuit or IC is a miniature, low cost electronic circuit consisting of active and passive components that are irreparably joined together on a single crystal chip of silicon. Most of the components used in ICs are not similar to conventional components in appearance although they perform similar electrical functions.

These circuits naturally offer a number of distinct advantages over those made by interconnecting discrete components. These may be listed as follows:

1. Miniaturization and hence increased equipment density

2. Cost reduction due to batch processing

3. Increased system reliability due to elimination of soldered joints

4. Improved functional performance (as it is possible to fabricate even complex circuits for better characteristics)

5. Matched devices

6. Increased operating speeds (due to the absence of parasitic capacitance effect)

7. Reduction in power consumption.

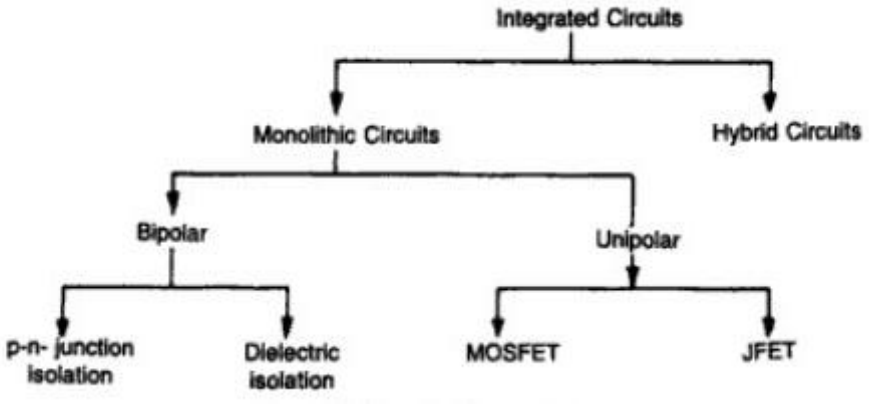
1.2 Classification of IC's

Integrated circuits offer a wide range of applications and could be broadly classified as:

- Digital ICs
- Linear ICs

Based upon the above requirements, two distinctly different IC technologies namely, Monolithic technology and Hybrid technology have been developed.

In monolithic integrated circuits, all circuit components, both active and passive elements and their interconnections are manufactured into or on top of a single chip of silicon. The monolithic circuit is ideal for applications where identical circuits are required in very large quantities and hence provides lowest per-unit cost and highest order of reliability. In hybrid circuits, separate component parts are attached to a ceramic substrate and interconnected by means of either metallization pattern or wire bonds.



1.3 Basic Information of op – amplifier 741 and its features

The circuit schematic of an op-amp is a triangle as shown in Fig. 1.1. It has two input terminals and one output terminal. The terminal with a (-) sign is called inverting input terminal and the terminal with (+) sign is called the non-inverting input terminal.

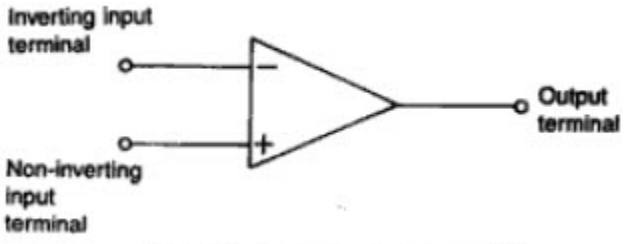


Figure 1.1

Op-amps have five basic terminals, that is, two input terminals, one output terminal and two power supply terminals. The significance of other terminals varies with the type of the op-amp. In case of DIP package of 741 shown in figure 1.2, the top pin on the left of the notch locates pin 1, has a dot on it for identification. The other pins are numbered counter-clockwise from pin 1. Pin 2 is called the inverting input terminal and pin 3 is the non-inverting input terminal, pin 6 is the output terminal and pins 7 and 4 are the power supply terminals labelled as V and V- respectively. Terminals 1 and 5 are used for de offset. The pin 8 marked NC indicates No Connection.

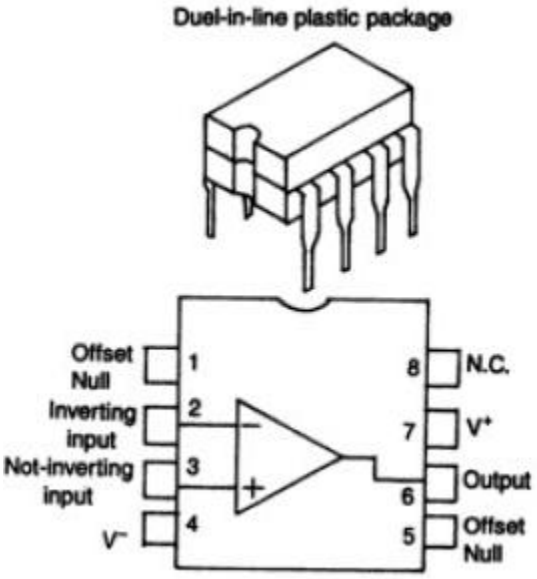


Figure 1.2 pin configuration of 8-pin DIP IC 741

1.4 The Ideal Operational amplifier

The schematic symbol of an op-amp is shown in Fig.1.3(a) It has two input terminals and one output terminal. Other terminals have not been shown for simplicity. The and + symbols at the input refer to inverting and non-inverting input terminals respectively, i.e if u1 = 0, output v is 180° out of phase with input signal ug. And, when v2 = 0, output v, will be in phase with the input signal applied at v1. This op-amp is said to be ideal if it has the following characteristics.

Open loop voltage gain, $A_{OL} = \infty$

Input impedance, R1 = ∞

Output impedance, $R_{o = 0}$

Bandwidth ,BW = ∞

Zero offset, i.e. v_o= 0 when $V_1 = V_2 = 0$.

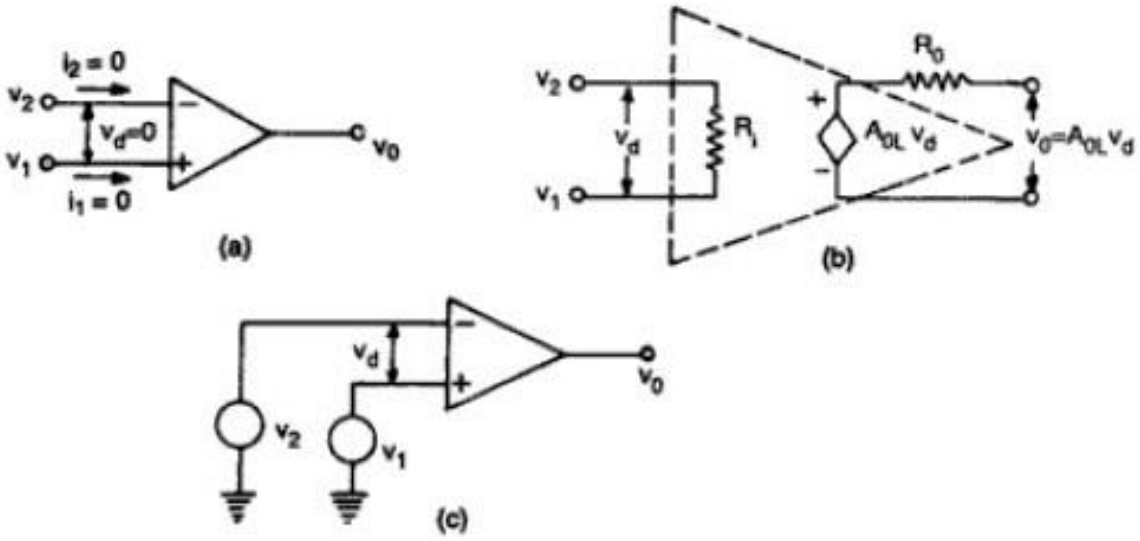


Figure 1.3

It can be seen that

(i) an ideal op-amp draws no current at both the input terminals i.e., i=0. Because of infinite input impedance, any signal source can drive it and there is no loading on the preceding driver stage.

(ii) Since gain is ∞, the voltage between the inverting and non- inverting terminals, i.e., differential input voltage V_a= (V_1-V_2) is essentially zero for finite output voltage v_0

(iii) The output voltage v_0, is independent of the current drawn from the output as R = 0. The output thus can drive an infinite number of other devices.

The above properties can never be realized in practice. However, the use of such an Ideal op-amp model simplifies the mathematics involved in op-amp circuits. There are practical op-amps that can be made to approximate some of these characteristics.

A physical amplifier is not an ideal one. So, the equivalent circuit of an op-amp may be shown in Fig. 1.3 (b) .

1.4.1 Open loop operation of op-amp 741

The simplest way to use an op-amp is in the open loop mode. Refer to Fig. 1.3 (c). The output assumes one of the two possible output states, that is, +Vsat or -Vsat and the amplifier acts as a switch only. This has a limited number of applications such as voltage comparator, zero crossing detector etc.

1.4.2 Feedback in op-amp

The utility of an op-amp can be greatly increased by providing negative feedback. The output in this case is not driven into saturation and the circuit behaves in a linear manner.

Two Important Negative Feedback Circuits

There are two basic feedback connections used. In order to understand the operation of these circuits, we make two realistic simplifying assumptions discussed earlier also.

- The current drawn by either of the input terminals (non-inverting and inverting) is negligible.
- The differential input voltage v_a between non-inverting and inverting input terminals is essentially zero.

1.4.3 Inverting Amplifier :

An *OP* amplifier can be operated as an inverting amplifier as shown in Fig. 1.4. An input signal v_{in} is applied through input resistor *Ri* to the minus input (inverting input). The output is fed back to the same minus input through feedback resistor *Rf*. The plus input (noninverting input) is grounded. Note that the resistor *Rf* provides the *negative feedback*. Since the input signal is applied to the inverting input (–), the output will be inverted (*i.e*. 180° out of phase) as compared to the input. Hence the name inverting amplifier.

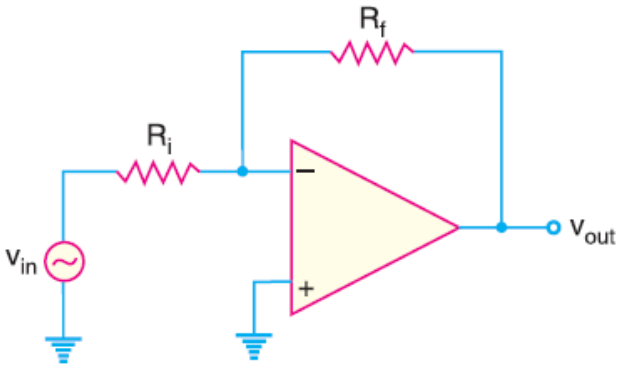


Figure 1.4

Voltage gain: An OP-amp has an infinite input impedance. This means that there is zero current at the inverting input. If there is zero current through the input impedance, then there must be *no* voltage drop between the inverting and non inverting inputs. This means that voltage at the inverting input (–) is zero (point *A*) because the other input (+) is grounded. The 0V at the inverting input terminal (point *A*) is referred to as **virtual ground.** This condition is illustrated in Fig.1.5. The point *A* is said to be at virtual ground because it is at 0V but is not physically connected to the ground (*i.e. VA* = 0*V*).

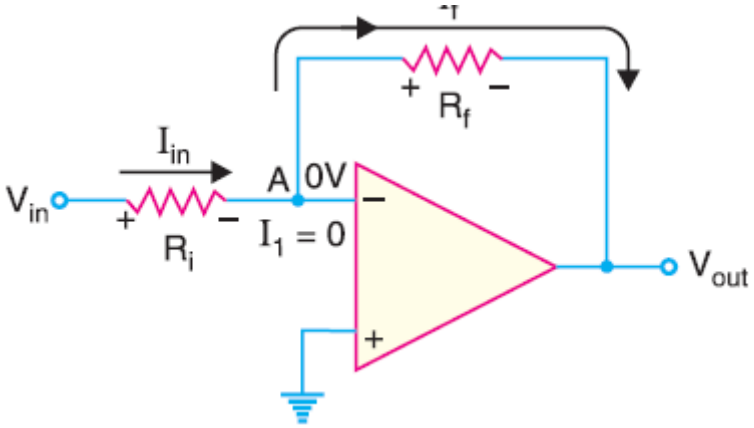


Figure 1.5

the current $I_{in,}$ the inverting input is zero. Therefore, current I_{in} flowing through *Ri* entirely flows through feedback resistor *Rf*. In other words, $I_f = I_{in}$

Now $I_{in} = \frac{Voltage\ across\ R_i}{R_i} = \frac{V_{in}}{R_i}$

$I_f = \frac{Voltage\ across\ R_f}{R_f} = \frac{-V_{out}}{R_f}$

Since $I_f = I_{in}$, $\frac{V_{in}}{R_i} = \frac{-V_{out}}{R_f}$

Voltage gain, $A_{CL} = \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_i}$

The output voltage is 180° out of phase with the input. Since the voltage drop across R_f is of the opposite polarity to the applied voltage, the circuit is providing negative feedback.

It is worthwhile to give a brief discussion about the input impedance and output impedance of inverting amplifier.

The negative sign indicates that output signal is inverted as compared to the input signal. The following points may be noted about the inverting amplifier :

The closed-loop voltage gain (A_{CL}) of an inverting amplifier is the ratio of the feedback resistance *Rf* to the input resistance *Ri*. *The closed-loop voltage gain is independent of the OP-amp's internal open-loop voltage gain.* Thus the negative feedback stabilises the voltage gain.

The inverting amplifier can be designed for unity gain. Thus if *Rf* = *Ri*, then voltage gain, $A_{CL} = -1$. Therefore, the circuit provides a unity voltage gain with 180° phase inversion.

If *Rf* is some multiple of *Ri*, the amplifier gain is constant. For example, if *Rf* = 10 *Ri*, then $A_{CL} = -10$ and the circuit provides a voltage gain of exactly 10 along with a 180° phase inversion from the input signal. If we select precise resistor values for *Rf* and *Ri*, we can obtain a wide range of voltage gains. *Thus the inverting amplifier provides constant voltage gain.*

(*i*) Input impedance. While an *OP*-amp has an extremely high input impedance, the inverting amplifier does not. As this figure 1.6 shows, the voltage source "sees" an input resistance (*Ri*) that is going to virtual ground. Thus the input impedance for the inverting amplifier is

Zi ~*Ri.*

The value of *Ri* will always be much less than the input impedance of the *OP*amp. Therefore, the overall input impedance of an inverting amplifier will also be much lower than the *OP*-amp input impedance.

(*ii*) Output impedance. Fig. 1.6 shows the inverting amplifier circuit. You can see from this figure that the output impedance of the inverting amplifier is the parallel combination of *Rf* and the output impedance of *OP*-amp itself. The presence of the negative feedback circuit reduces the output impedance of the amplifier to a value that is less than the output impedance of *OP*-amp.

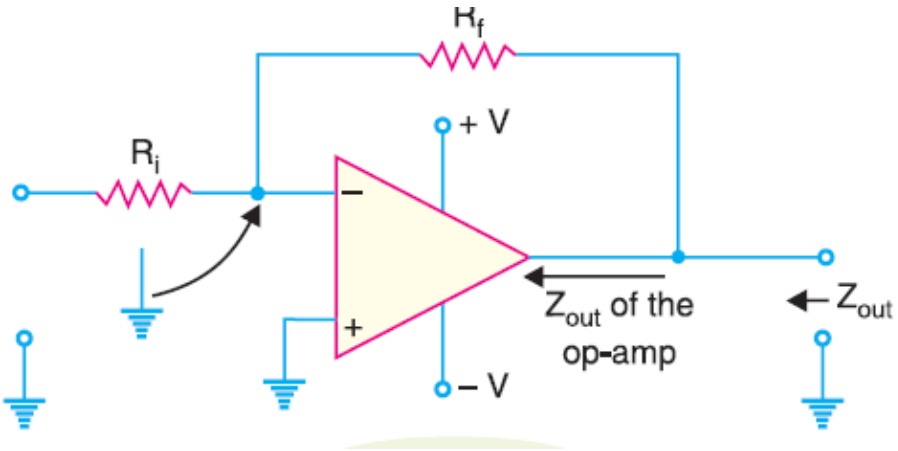


Figure 1.6

1.4.4 Non-inverting amplifier

There are times when we wish to have an output signal of the same polarity as the input signal. In this case, the *OP*-amp is connected as non inverting amplifier as shown in Fig. 1.7 . The input signal is applied to the non inverting input (+). The output is applied back to the input through the feedback circuit formed by feedback resistor *Rf* and input resistance *Ri*. Note that resistors *Rf* and *Ri* form a voltage divide at the inverting input (–).This produces **negative feedback* in the circuit. Note that *Ri* is grounded. Since the input signal is applied to the non inverting input (+), the output signal will be non inverted i.e., the output signal will be in phase with the input signal. Hence, the name non-inverting amplifier.

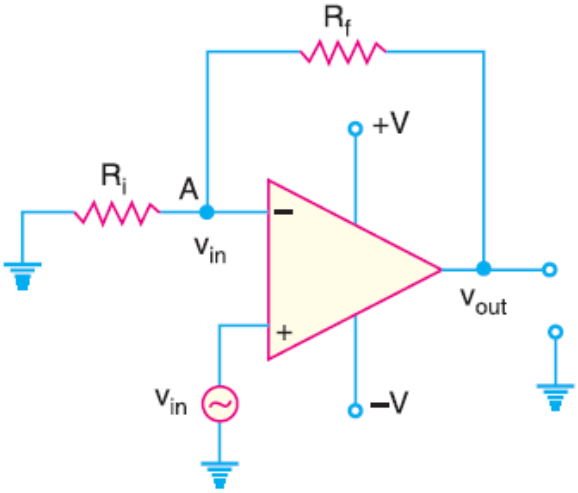


Figure 1.7

Voltage gain. If we assume that we are not at saturation, the potential at point *A* is the same as

Vin. Since the input impedance of *OP*-amp is very high, all of the current that flows through *Rf* also flows through *Ri*. Keeping these things in mind, we have,

Voltage across $R_i = V_{in} - 0$; Voltage across $R_f = V_{out} - V_{in}$

Now, Current through R_i = Current through R_f

$$\frac{V_{in} - 0}{R_i} = \frac{V_{out} - V_{in}}{R_f}$$

$$\frac{V_{out}}{V_{in}} = 1 + \frac{R_f}{R_i}$$

Voltage gain, $A_{CL} = \frac{V_{out}}{V_{in}} = 1 + \frac{R_f}{R_i}$

The following points may be noted about the noninverting amplifier:

$A_{CL} = \frac{V_{out}}{V_{in}} = 1 + \frac{R_f}{R_i}$, The voltage gain of noninverting amplifier also depends upon the values of *Rf* and *Ri*.

The voltage gain of a non inverting amplifier can be made equal to or greater than 1.

The voltage gain of a non inverting amplifier will always be greater than the gain of an equivalent inverting amplifier by a value of 1. If an inverting amplifier has a gain of 150, the equivalent non inverting amplifier will have a gain of 151.

The voltage gain is positive. This is not surprising because output signal is in phase with the input signal.

1.4.5 Voltage follower

The voltage follower arrangement is a special case of non inverting amplifier where all of the output voltage is fed back to the inverting input as shown in Fig. 1.8. Note that we remove *Ri*

and *Rf* from the non inverting amplifier and short the output of the amplifier to the inverting input. The voltage gain for the voltage follower is calculated as given below

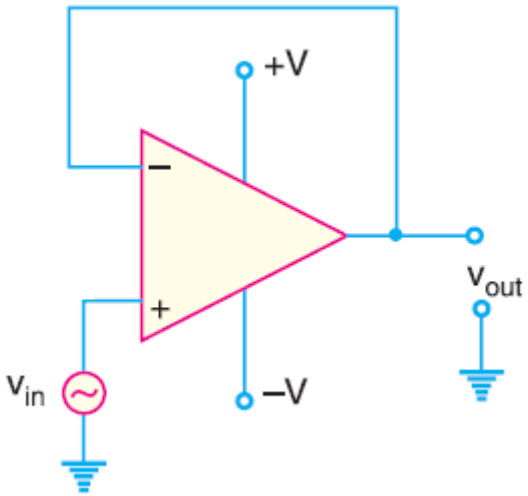


Figure 1.8

$$A_{CL} = 1 + \frac{R_f}{R_i} = 1 + \frac{0}{R_i} = 1 \qquad (R_f = 0\Omega)$$

Thus the closed-loop voltage gain of the voltage follower is 1. The most important features of the voltage follower configuration are its *very high input impedance* and its *very low output impedance.* These features make it a nearly ideal buffer amplifier to be connected between high-impedance sources and low-impedance loads.

1.5 Op-Amp internal circuit

Commercial IC op-amps usually consist of four cascaded blocks as shown in Fig.1.9. The first two stages are cascaded differential amplifiers used to provide high gain and high input resistance. The third stage acts as a buffer as well as a level shifter. The buffer is usually an emitter follower whose input impedance is very high so that it prevents loading of the high gain stage. The level shifter adjusts the d.c. voltages so that output voltage is zero for zero inputs. The adjustment of d.c. level is required as the gain stages are direct coupled. As it is not possible to fabricate large value of capacitors, all ICs are direct coupled usually. The output stage is designed to provide a low output impedance as demanded by the ideal op-amp characteristics.

The output voltage should swing symmetrically with respect to ground. To allow such symmetrical swing, the amplifier is provided with both positive and negative supply voltages. Power supply voltages of + 15V are common. Additionally, an op-amp generally incorporates circuitry to provide drift compensation and frequency compensation

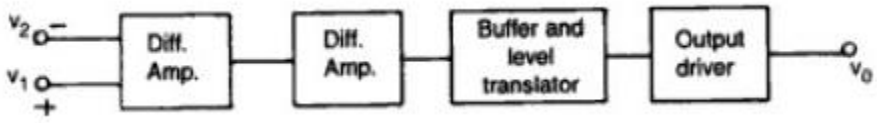


Figure 1.9

1.5.1 Differential amplifier

Since differential amplifier (*DA*) is key to the operation of *OP*-Amp, we shall discuss this circuit in detail. So far we have considered general-purpose amplifiers. In these conventional amplifiers, the signal (generally single input) is applied at the input terminals and amplified output is obtained at the output terminals. However, we can design an amplifier circuit that accepts two input signals and amplifies the difference between these two signals. Such an amplifier is called a *differential amplifier* (*DA*). *A* **differential amplifier** is a circuit that can accept two input signals and amplify the difference between these two input signals. There are two input voltages V_1 and V_2. This amplifier amplifies the difference between the two input voltages. Therefore, the output voltage is $V_o = A (V_1 - V_2)$ where A is the voltage gain of the amplifier.

1.5.2 Internal circuit of Differential Amplifier

The basic circuit of a differential amplifier is shown in Fig. 1.10 (*i*). It consists of two transistors *Q*1 and *Q*2 that have identical (ideally) characteristics. They share a common positive supply *VCC*, common emitter resistor *RE* and common negative supply *VEE*. Note that the circuit is symmetrical. Fig.1.10 (*ii*) shows the symbol of differential amplifier.

The following points may be noted about the differential amplifier :

(*i*) The differential amplifier (*DA*) is a two-input terminal device using atleast two transistors. There are two output terminals marked 1 (*v*out 1) and 2(*v*out 2).

(*ii*) The *DA* transistors *Q*1 and *Q*2 are matched so that their characteristics are the same. The collector resistors (*RC1* and *RC2*) are also equal. The equality of the matched circuit components makes the *DA* circuit arrangement completely symmetrical.

(*iii*) We can apply signal to a differential amplifier (*DA*) in the following two ways :

(*a*) The signal is applied to one input of *DA* and the other input is grounded. In that case, it is called *single-ended input* arrangement.

(*b*) The signals are applied to both inputs of *DA*. In that case, it is called *dual-ended* or *double-ended input* arrangement.

(*iv*) We can take output from *DA* in the following two ways :

(*a*) The output can be taken from one of the output terminals and the ground. In that case, it is called *single-ended output* arrangement.

(*b*) The output can be taken between the two output terminals (*i.e*., between the collectors of *Q*1 and *Q*2). In that case, it is called *double-ended output* arrangement or *differential output*.

(*v*) *Generally, the differential amplifier (DA) is operated for single-ended output*. In other words, we take the output either from output terminal 1 and ground or from output terminal 2 and ground. Any input/output terminal that is grounded is at *0V*.

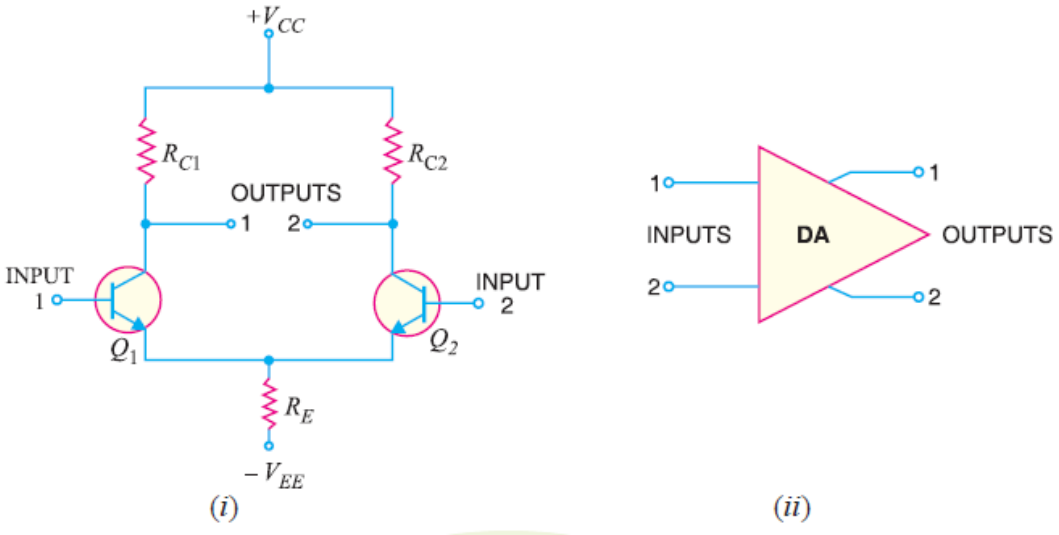


Figure 1.10

1.5.3 Common-mode and Differential-mode Signals

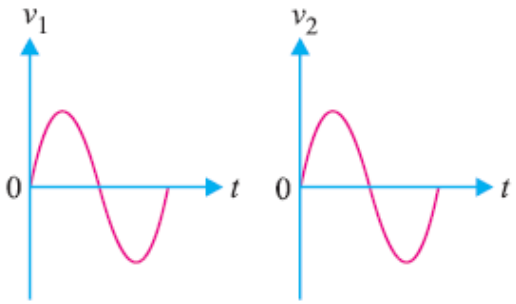
The importance of a differential amplifier lies in the fact that the outputs are proportional to the *difference* between the two input signals. Thus the circuit can be used to amplify the difference between the two input signals or amplify only one input signal simply by grounding the other input.

The input signals to a *DA* are defined as :

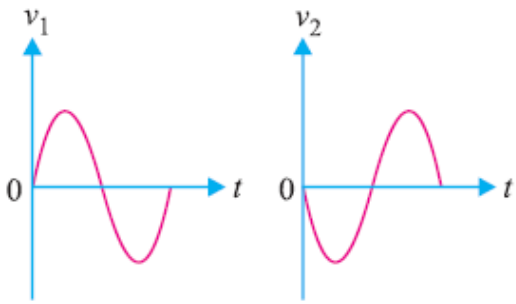
(*i*) Common-mode signals **(*ii*)** Differential-mode signals

(*i*) Common-mode signals : When the input signals to a *DA* are in phase and exactly equal in amplitude, they are called *common-mode signals* The common-mode signals are rejected (not amplified) by the differential amplifier. It is because a differential amplifier amplifies the difference between the two signals (V_1 - V_2) and for common-mode signals, this difference is zero. Note that for common-mode operations, $v_1 = v_2$.

(*ii*) Differential-mode signals. When the input signals to a *DA* are 180° out of phase and exactly equal in amplitude, they are called differential-mode signals. The differential-mode signals are amplified by the differential amplifier. It is because the difference in the signals is twice the value of each signal. For differential-mode signals, $v_1 = -v_2$.



Common-mode signals



Differential-mode signals

1.5.4 Voltage Gains of DA

The voltage gain of a DA operating in differential mode is called differential-mode voltage gain and is denoted by A_{dm}. The voltage gain of DA operating in common-mode is called common-mode voltage gain and is denoted by A_{cm} Ideally, a DA provides a very high voltage gain for differential-mode signals and zero gain for common-mode signals. However, practically, differential amplifiers do exhibit a very small common-mode gain (usually much less than 1) while providing a high differential voltage gain (usually several thousands). The higher the differential gain w.r.t. the common-mode gain, the better the performance of the DA in terms of rejection of common-mode signals.

1.5.5 Common Mode Rejection Ratio (CMRR)

A differential amplifier should have high differential voltage gain (A_{dm}) and very low common mode voltage gain (A_{cm}). The ratio A_{dm} / A_{cm} is called common-mode rejection ratio (*CMRR*)

CMRR = $\frac{A_{DM}}{A_{CM}}$ Very often, the *CMRR* is expressed in decibels (*dB*). The decibel measure for *CMRR* is given by;

$$CMRR_{dB} = 20\log_{10} CMRR$$

1.6 Op-Amp.Characteristics

Earlier we have used an ideal op-amp, and assumed that the op-amp responds equally well to both ac and de input voltages. However, a practical op-amp does not behave this way. A practical op-amp has some de voltage at the output even with both the inputs grounded. The factors responsible for this and the suitable compensating techniques are discussed. Also, under ac conditions the characteristics of an op-amp are frequency dependent. The limitations of an op-amp under ac conditions and methods of compensation are discussed.

1.6.2 DC CHARACTERISTICS

An ideal op-amp draws no current from the source and its response is also independent of temperature. However, a real op-amp does not work this way. Current is taken from the source

into the op-amp inputs. Also the two inputs respond differently to current and voltage due to mismatch in transistors. A real op-amp also shifts its operation with temperature. These non-ideal dc characteristics that add error components to the de output voltage are:

- Input bias current
- Input offset current
- Input offset voltage
- Thermal drift.

1.6.2.1 Input bias current

The inputs to an OP- amp require some amount of d.c. biasing current for the transistors in the differential amplifier. The *input bias current* is defined as the average of the two d.c. base currents.

$$I_{in(bias)} = \frac{I_{B1} + I_{B2}}{2}$$

For example, if I_{B1} = 85 μA and I_{B2}= 75 μA, then the input bias current is 80μA. This means that when no signal is applied, the inputs of *OP*- amp (*i.e*., *DA*) will draw a d.c. current of 80 μA. The fact that both transistors in the differential amplifier require an input biasing current leads to the following operating restriction : *An OP- amp will not work if either of its inputs is open.* For example, look at the circuit shown in Fig. 1.11. The non-inverting input is shown to have an open between the OP- amp and ground. The open circuit would not allow the d.c. biasing current required for the operation of the differential amplifier (*The transistor associated with the inverting input would work but not the one associated with the non-inverting input*). Since the differential amplifier would not work, the overall *OP*-amp circuit would not work. Thus an input bias current path must always be provided for *both OP*-amp inputs.

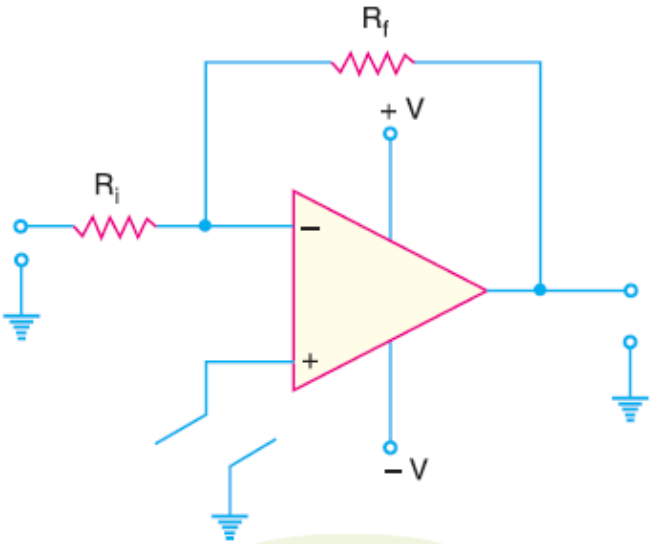


Figure 1.11

1.6.2.2 Input offset current

When the output offset voltage of a *DA* (or *OP*- amp) is eliminated, there will be a slight difference between the input currents to the non inverting and inverting inputs of the device. This slight difference in input currents is called *input offset current* and is caused by a beta (β) mismatch between the transistors in the differential amplifier. As an example, suppose I_{B1} = 75 μA and I_{B2} = 65 μA. Then, $I_{in(offset)}$ = 75 – 65 = 10 μA .The difference in the base currents indicates how closely matched the transistors are. If the transistors are identical, the input offset current is zero because both base currents will be equal. But in practice, the two transistors are different and the two base currents are not equal.

1.6.2.3 Input offset voltage :

There are several methods that may be used to eliminate output offset voltage. One of these is to apply an *input offset voltage* between the input terminals of *DA* (or *OP*- amp) so as to make output 0*V* as shown in Fig.1.12. The value of input offset voltage (*Vi*0) required to eliminate the output offset voltage is given by;

$$V_{io} = \frac{V_{output(offset)}}{A}$$

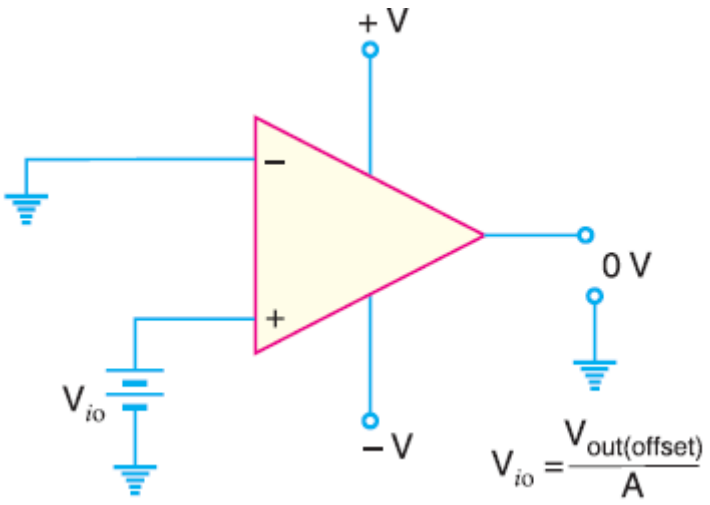


Figure 1.12

1.6.2.4 Thermal drift

Bias current, offset current and offset voltage change with temperature. A circuit carefully nulled at 25°C may not remain so when the temperature rises to 35°C. This is called drift. Often, offset current drift is expressed in nA/°C and offset voltage drift in mV/°C. These indicate the change in offset for each degree celsius change in temperature.There are very few circuit techniques that can be used to minimize the effect of drift. Careful printed circuit board layout must be used to keep op-amps away from source of heat. Forced air cooling may be used to stabilize the ambient temperature.

UNIT – II APPLICATIONS OF OPERATIONAL AMPLIFIERS

LINEAR APPLICATIONS OF OP-AMP: Solution to simultaneous equations and differential equations, Instrumentation amplifiers, V to I and I to V converters.

NON-LINEAR APPLICATIONS OF OP-AMP: Sample and Hold circuit, Log and Antilog amplifier, multiplier and divider, Comparators, Schmitt trigger, Multivibrators, Triangular and Square waveform generators.

2.1 Linear applications of op-amp:

2.1.1 Solution to simultaneous equations and differential equations

Let us now see how an analog computer can be used to solve a second order differential equation given as

$$\frac{d^2y}{dt^2} + 5.4\frac{dy}{dt} + 0.58y = u(t)$$

With initial conditions y(0) = -4.8 and $\dot{y}(0) = 2.3$

Rewrite Equation by keeping the highest order derivative on the left hand side and taking all other terms to the right side as

$\ddot{y}$ = -5.4$\dot{y}$ -0.58 y + u(t)

Assuming $\ddot{y}$ is available, it may be successively integrated to obtain y and y as shown in Fig. 2.1 At the output of amplifier 4. i.e., point B, we obtain the sum -5.4$\dot{y}$ -0.58y+u(t) which is precisely equal to y with which we started . Thus points A and B may be connected together to get the computer set-up for solving the given differential equation. The initial conditions y(0)=-4.8 and $\dot{y}(0) = 2.3$ have to be placed in the computer set-up with the V as required and potentiometer. One has to be careful about the polarity of the reference voltage for setting up the initial condition

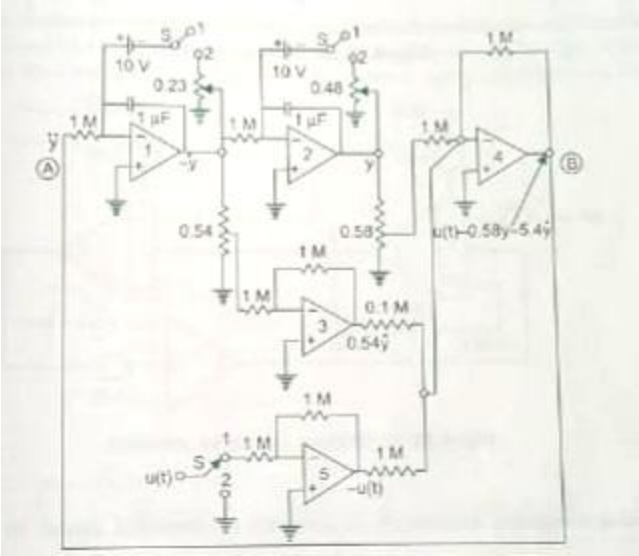


Figure 2.1

The initial conditions are first established by putting the switch S in position 2. With S in position 1, the solution is obtained at the output terminal to which a CRO or plotter is connected.

Solving simultaneous equations

A set of simultaneous equations in two unknowns can also be solved using analog simulation. Consider two first order differential equations:

$$\frac{dx}{dt} = -a_1 x - b_1 y + c_1 f$$

$$\frac{dy}{dt} = -a_2 x - b_2 y + c_2 f$$

where x and y are unknown variables. f is the input and all coefficients are known constants. Equations may be simulated separately as shown in Figs. 2.2 (a) and (b) Now interconnect the two systems to get the unknown x and y as shown in Fig.2.2 (c)

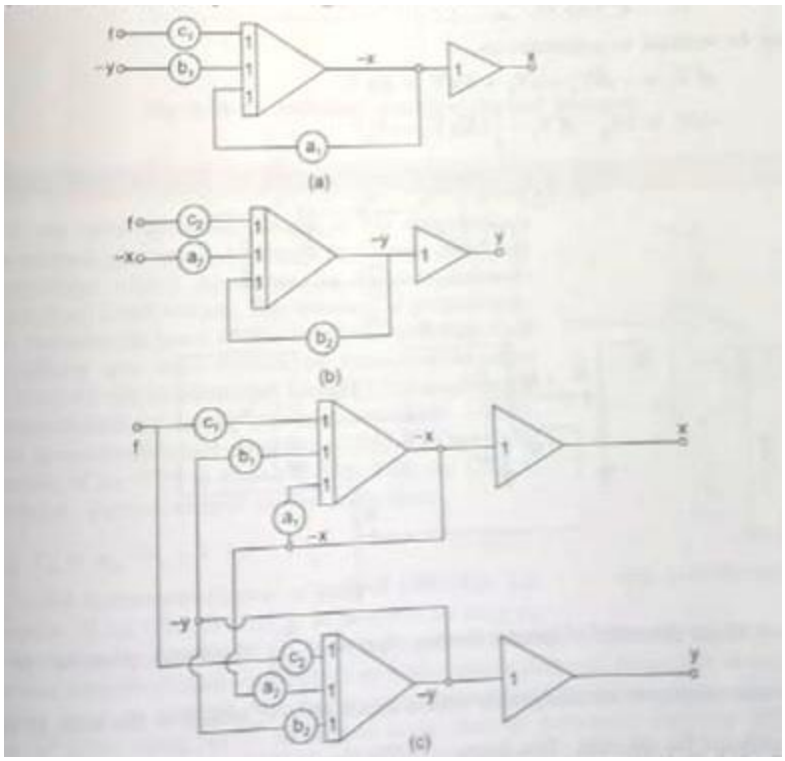


Figure 2.2

2.1.2 Instrumentation Amplifiers:

Instrumentation amplifiers are commonly used in environments with high common mode noise such as in data acquisition systems where remote sensing of input variables is required. An **instrumentation amplifier** is a differential voltage-gain device that amplifies the difference between the voltages existing at its two input terminals. The main purpose of an instrumentation amplifier is to amplify small signals that may be riding on large common mode voltages. The key characteristics are high input impedance, high common-mode rejection, low output offset, and low output impedance. The basic instrumentation amplifier is an integrated circuit that internally has three operational amplifiers and several resistors. The voltage gain is usually set with an external resistor. A basic instrumentation amplifier is shown in Figure 2.3. Op-amps A1 and A2 are non inverting configurations that provide high input impedance and voltage gain. Op-amp A3 is used as a unity-gain differential amplifier with high-precision resistors that are all equal in value ($R3 = R4 = R5 = R6$).

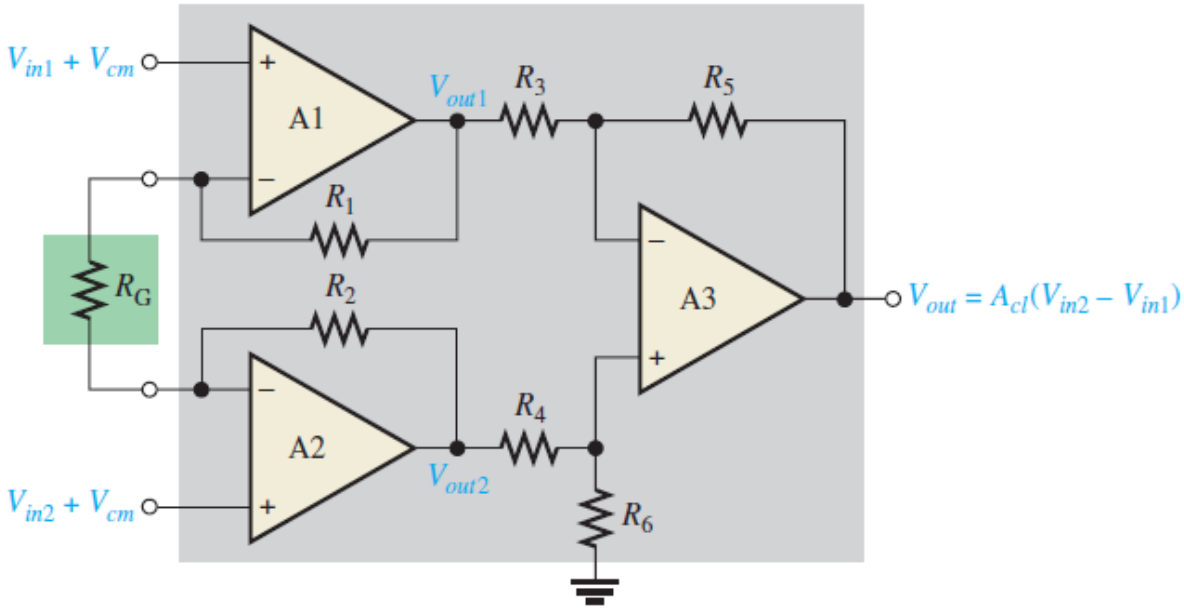


Figure 2.3

The gain-setting resistor, *R*G, is connected externally as shown in Figure 14–2. Op-amp A1 receives the differential input signal *Vin*1 on its non inverting (+) input and amplifies this signal with a voltage gain of

$$Av = 1 + \frac{R_1}{R_G}$$

Op-amp A1 also has *Vin*2 as an input signal to its inverting (-) input through op-amp A2 and the path formed by *R*2 and *R*G. The input signal *Vin*2 is amplified by op-amp A1 with a voltage gain of

$$Av = \frac{R_1}{R_G}$$

The overall closed-loop gain of the instrumentation amplifier is

$$Av = 1 + \frac{2R_1}{R_G}$$

2.1.3 Voltage to current converters and current to voltage converters

Voltage-to-Current Converter

A basic voltage-to-current converter is shown in Figure 2.4 Like the OTA, this circuit can be used in applications where it is necessary to have an output (load) current that is controlled by an input voltage. A drawback to this circuit is that the load is not grounded. Neglecting the input offset voltage, both inverting and non inverting input terminals of the op amp are at the same voltage, *Vin*. Therefore, the voltage across *R*1 equals *Vin*. Since there is negligible current at the inverting input, the current through *R*1 is the same as the current through *RL*; thus

$$I_L = \frac{V_{in}}{R_1}$$

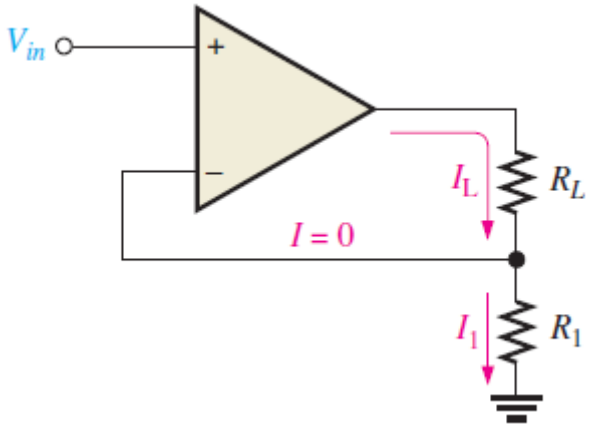


Figure 2.4

Current-to-Voltage Converter

A current-to-voltage converter converts a variable input current to a proportional output voltage. A basic circuit that accomplishes this is shown in Figure 2.5. Since practically all of *Ii* is through the feedback path, the voltage dropped across *Rf* is I_1 Rf.Because the left side of *Rf* is at virtual ground (0 V), the output voltage equals the voltage across *Rf*, which is proportional to *Ii*.

$$\boldsymbol{Vout = I_1\, Rf}$$

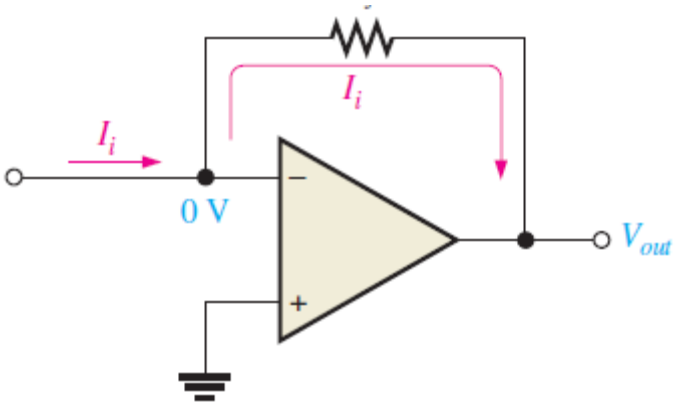
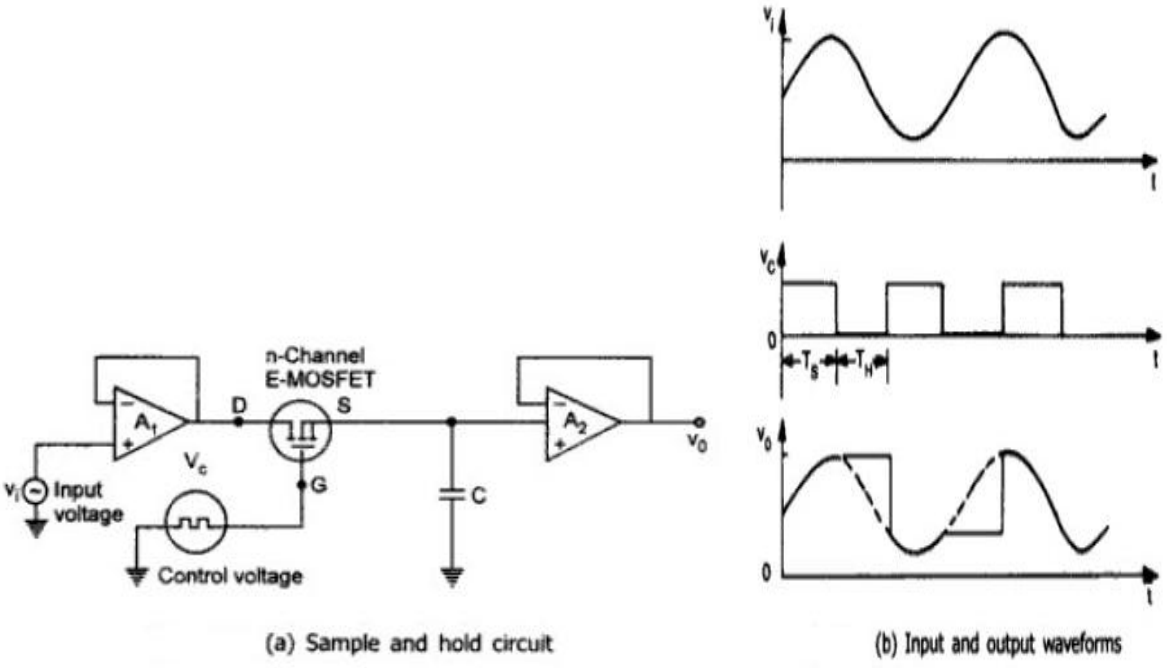


Figure 2.5

2.2 Non linear Applications of Op-amp

2.2.1 Sample and Hold

A sample and hold circuit samples an input signal and holds on to its last sampled value until the input is sampled again. This type of circuit is very useful in digital interfacing and analog to digital and pulse code modulation systems. One of the simplest practical sample and hold circuit configuration is shown in Fig.2.5 (a). The n-channel E-MOSFET works as a switch and is controlled by the control voltage v, and the capacitor C stores the charge. The analog signal v; to be ampled is applied to the drain of E-MOSFET and the control voltage v, is applied to its gate. When v, is positive, the E-MOSFET turns on and the capacitor C charges to the instantaneous value of input v with a time constant [(R +r $_{ps(on)}$.)C] Here R, is the output resistance of the voltage follower A, and r $_{ps(on)}$ is the resistance of the MOSFET when on. Thus the input voltage v, appears across the capacitor C and then at the output through the voltage follower A2. The waveforms are as shown in Fig. 2.5 (b). During the time when control voltage v, is zero, the E-MOSFET is off. The capacitor C is now facing the high input impedance of the voltage follower A, and hence cannot discharge. The capacitor holds the voltage across it. The time period Tg, the time during which voltage across the capacitor is equal to input voltage is called sample period. The time period Ty of v, during which the voltage across the capacitor is held constant is called hold period. The frequency of the control voltage should be kept higher than (at least twice) the input so as to retrieve the input from output waveform. A low leakage capacitor such as Polystyrene, Mylar, or Teflon should be used to retain the stored charge



(a) Sample and hold circuit (b) Input and output waveforms

Figure 2.5

2.2.2 Log and Antilog Amplifiers

Log amplifier

The fundamental log-amp circuit is shown in Fig. 2.6 (a) where a grounded base transistor is placed in the feedback path. Since the collector is held at virtual ground and the base is also grounded, the transistor's voltage-current relationship becomes that of a diode and is given by,

$$I_E = I_s (e^{qV_E/kT} - 1)$$

Since, $I_C = I_E$ for a grounded base transistor,

$$I_C = I_s (e^{qV_E/kT} - 1)$$

I_s = emitter saturation current $\approx 10^{-13}$ A
k = Boltzmann's Constant
T = absolute temperature (in °K)

Therefore, $$\frac{I_C}{I_s} = (e^{qV_E/kT} - 1)$$

or, $$e^{qV_E/kT} = \frac{I_C}{I_s} + 1$$

$$= \frac{I_C}{I_s} \qquad [\text{as } I_s = 10^{-13} \text{ A}, I_C >> I_s]$$

Taking natural log on both sides, we get

$$V_E = \frac{kT}{q} \ln\left(\frac{I_C}{I_s}\right)$$

Also in Fig. 2.6 (a), $I_C = \frac{V_i}{R_1}$

$$V_E = -V_o$$

so,
$$V_o = -\frac{kT}{q}\ln\left(\frac{V_i}{R_1 I_s}\right) = -\frac{kT}{q}\ln\left(\frac{V_i}{V_{ref}}\right)$$

where
$$V_{ref} = R_1 I_s$$

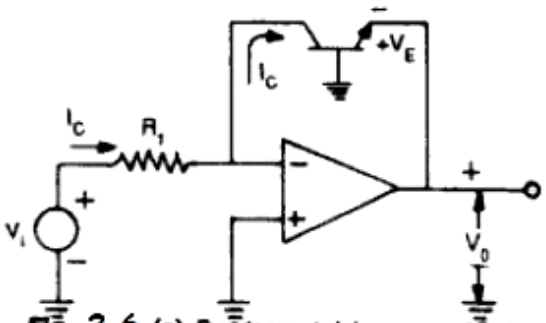


Fig. 2.6 (a) Fundamental log-amp circuit

The output voltage is thus proportional to the logarithm of input voltage. Although the circuit gives natural log (ln), one can find $\log_{10}$ by proper scaling

$$\log_{10} X = 0.4343 \ln X$$

The circuit, however, has one problem. The emitter saturation current I_s varies from transistor to transistor and with temperature. Thus a stable reference voltage V_{ref} cannot be obtained. This is eliminated by the circuit given in Fig. 2.6 (b). The input is applied to one log-amp, while a reference voltage is applied to another log-amp. The two transistors are integrated close together in the same silicon wafer. This provides a close match of saturation currents and ensures good thermal tracking.

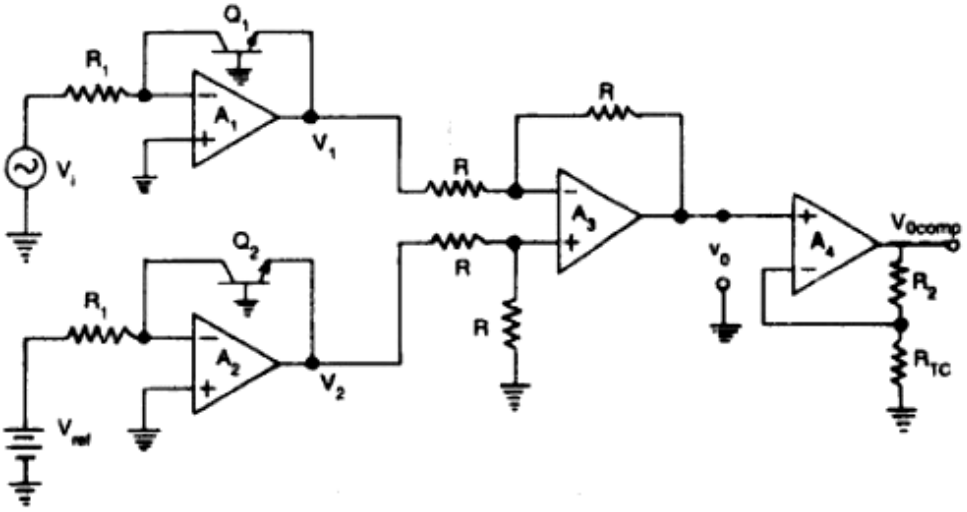


Fig. 2.6 (b) Log-amp with saturation current and temperature compensation

Assume, $I_{s1} = I_{s2} = I_s$

and then, $$V_1 = -\frac{kT}{q} \ln\left(\frac{V_i}{R_1 I_s}\right)$$

and $$V_2 = -\frac{kT}{q} \ln\left(\frac{V_{ref}}{R_1 I_s}\right)$$

Now, $$V_o = V_2 - V_1 = \frac{kT}{q}\left[\ln\left(\frac{V_i}{R_1 I_s}\right) - \ln\left(\frac{V_{ref}}{R_1 I_s}\right)\right]$$

or, $$V_o = \frac{kT}{q} \ln\left(\frac{V_i}{V_{ref}}\right)$$

Thus reference level is now set with a single external voltage source. Its dependence on device and temperature has been removed. The voltage V_o is still dependent upon temperature and is directly proportional to T. This is compensated by the last op-amp stage A_4 which provides a non-inverting gain of $(1 + R_2/R_{TC})$. Now, the output voltage is,

$$V_{o\ comp} = \left(1 + \frac{R_2}{R_{TC}}\right)\frac{kT}{q} \ln\left(\frac{V_i}{V_{ref}}\right)$$

where R_{TC} is a temperature-sensitive resistance with a positive coeffecient of temperature (sensistor) so that the slope of the equation becomes constant as the temperature changes.

Antilog amplifier

The circuit is shown in Fig. 2.7 The input V_i for the antilog-amp is fed into the temperature compensating voltage divider R_2 and R_{TC} and then to the base of Q_2. The output V_o of the antilog-amp is fed back to the inverting input of A_1 through the resistor R_1. The base to emitter voltage of transistors Q_1 and Q_2 can be written as

$$V_{Q1\ B\text{-}E} = \frac{kT}{q} \ln\left(\frac{V_o}{R_1 I_s}\right)$$

and

$$V_{Q2\ B\text{-}E} = \frac{kT}{q} \ln\left(\frac{V_{ref}}{R_1 I_s}\right)$$

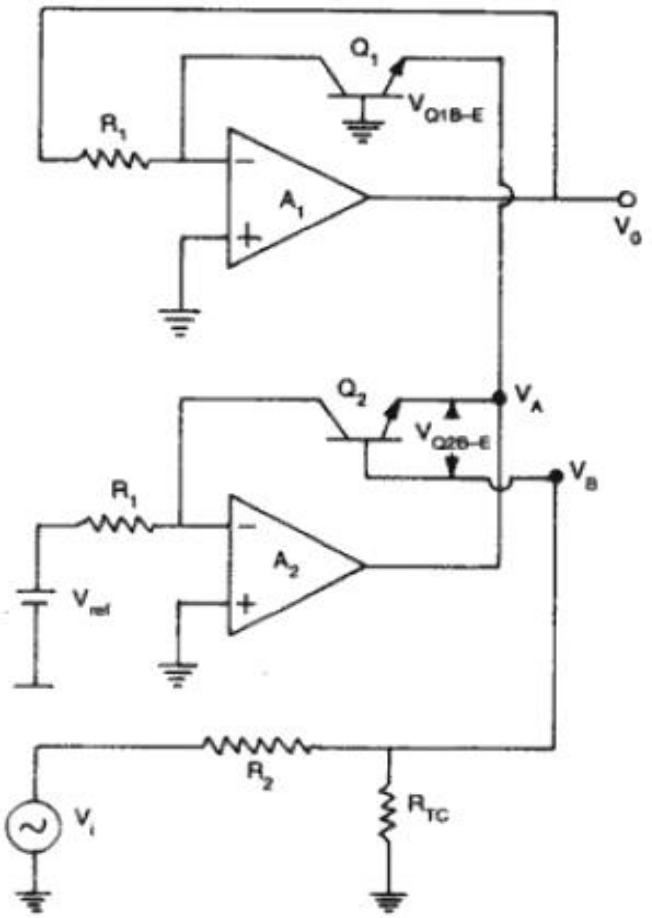


Fig. 2.7 Antilog amplifier

Since the base of Q_1 is tied to ground, we get

$$V_A = -V_{Q1\ B\text{-}E} = -\frac{kT}{q}\ln\left(\frac{V_o}{R_1 I_s}\right)$$

The base voltage V_B of Q_2 is

$$V_B = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right)V_i$$

The voltage at the emitter of Q_2 is

$$V_{Q2\ E} = V_B + V_{Q2\ E\text{-}B}$$

or,
$$V_{Q2\ E} = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right)V_i - \frac{kT}{q}\ln\left(\frac{V_{ref}}{R_1 I_s}\right)$$

But the emitter voltage of Q_2 is V_A, that is,

$$V_A = V_{Q2\ E}$$

or,
$$-\frac{kT}{q}\ln\frac{V_o}{R_1 I_s} = \frac{R_{TC}}{R_2 + R_{TC}}V_i - \frac{kT}{q}\ln\frac{V_{ref}}{R_1 I_s}$$

or,
$$\frac{R_{TC}}{R_2 + R_{TC}}V_i = -\frac{kT}{q}\left(\ln\frac{V_o}{R_1 I_s} - \ln\frac{V_{ref}}{R_1 I_s}\right)$$

or,
$$-\frac{q}{kT}\frac{R_{TC}}{R_2 + R_{TC}}V_i = \ln\left(\frac{V_o}{V_{ref}}\right)$$

Changing natural log, i.e., ln to $\log_{10}$

$$-0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right)V_i = 0.4343 \times \ln\left(\frac{V_o}{V_{ref}}\right)$$

or,
$$-K'V_i = \log_{10}\left(\frac{V_o}{V_{ref}}\right)$$

or,
$$\frac{V_o}{V_{ref}} = 10^{-K'V_i}$$

or,
$$V_o = V_{ref}\,(10^{-K'V_i})$$

where
$$K' = 0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right)$$

Hence an increase of input by one volt causes the output to decrease by a decade.

2.2.3 Multiplier and divider

Multiplier

There are a number of applications of analog multiplier such as frequency doubling, frequency shifting, phase angle detection, real power computation, multiplying two signals, dividing and squaring of signals. A basic multiplier schematic symbol is shown in Fig. 2.8 (a). Two signal inputs (v_x and v_y) are provided. The output is the product of the two inputs divided by a reference voltage V_{ref}.

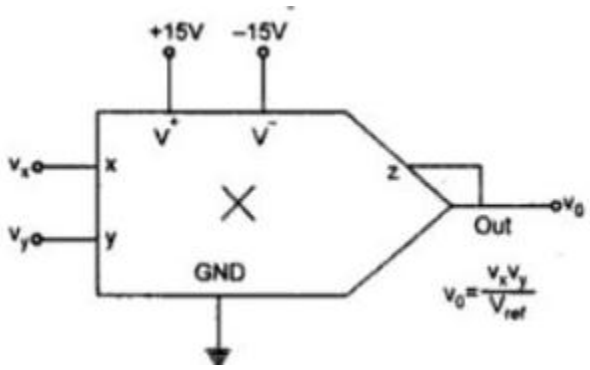


Figure 2.8(a)

$$V_o = \frac{v_x \ v_y}{v_{ref}}$$

$v_x < v_{ref}$ or

$v_y < v_{ref}$

the output of the multiplier will not saturate. If both inputs are positive, the IC is said to be a one quadrant multiplier. A two quadrant multiplier will function properly if one input is held positive and the other is allowed to swing both positive and negative. If both inputs may be either positive or negative, the IC is called a four quadrant multiplier.

Divider

Division, the complement of multiplication, can be accomplished by placing the multiplier circuit element in the op-amp& feedback loop. The output voltage from the divider in Fig. 2.8(b) with input signals v_x and v_y as dividend and divisor respectively, is given by

$$V_o = - \frac{v_{ref}\ v_y}{v_x}$$

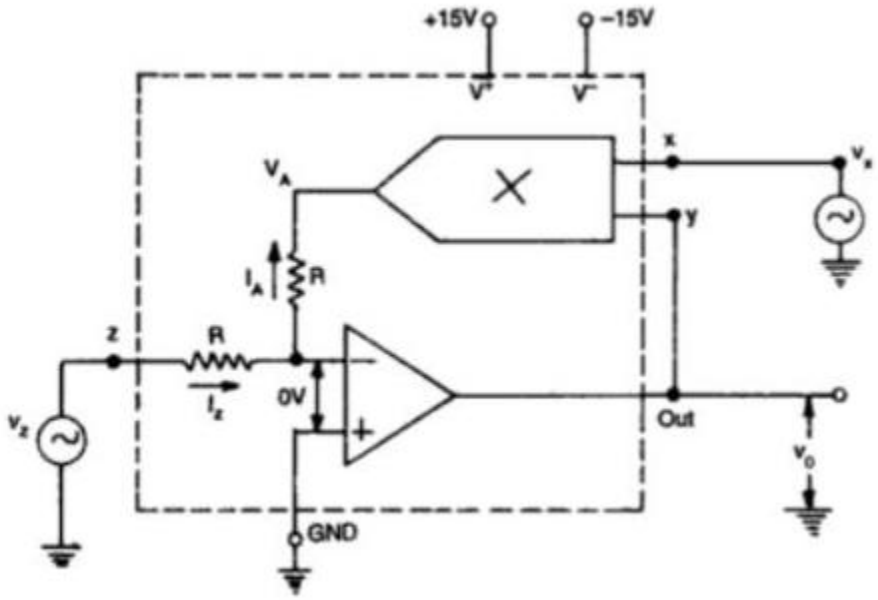


Figure 2.8(b)

Division by zero is, of course, prohibited. Multiplier IC can be used for squaring a signal. Similarly, divider circuit can be used to take the square root of a signal.

2.2.4 Comparator

A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input. It is basically an open-loop op-amp with output ± Vsat (= Vcc) as shown in the ideal transfer characteristics of Fig.2.9 (a). However, a commercial op-amp has the transfer characteristics of Fig.2.9 (b).

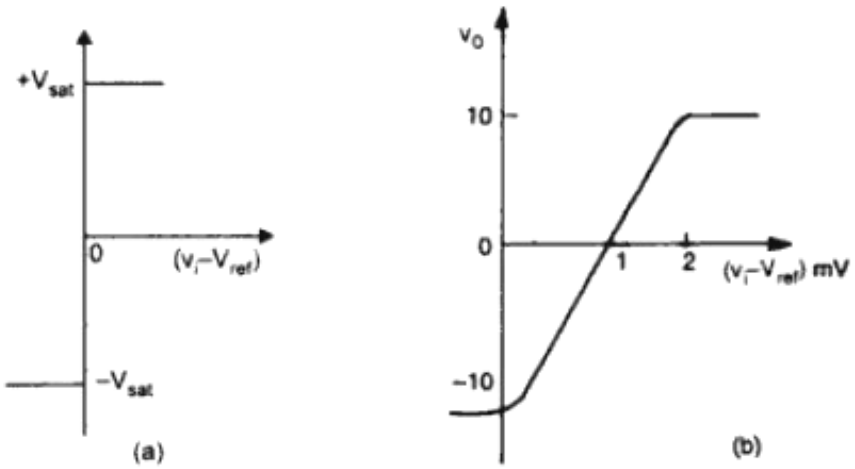


Figure 2.9

It may be seen that the change in the output state takes place with an increment in input u, of only 2 mV. This is the uncertainty region where output cannot be directly defined. There are basically two types of comparators:

- Non-inverting comparator
- Inverting comparator.

The circuit of Fig.2.10 (a) is called a non-inverting comparator. A fixed reference voltage V_{ref} is applied to (-) input and a time varying signal v_{in} is applied to (+) input. The output voltage is at -Vsat for $v_{in} < v_{ref}$. The output waveform for a sinusoidal input signal applied to the (+) input is shown in Fig. 2.10 (b and c) for positive and negative Vref respectively.

In a practical circuit Ver is obtained by using a 10 k potentiometer which forms a voltage divider with the supply voltages V+ and V- with the wiper connected to (-) input terminal as shown in Fig.2.10 (d). Thus a Vref of desired amplitude and polarity can be obtained by simply adjusting the 10 k potentiometer.

Figure 2.11 (a) shows a practical inverting comparator in which the reference voltage Vref is applied to the (+) input and u, is applied to (-) input. For a sinusoidal input signal, the output waveform is shown in Fig.2.11 (b) and (c) for V_{ref} positive and negative respectively.

Output voltage levels independent of power supply voltages can also be obtained by using a resistor R and two back to back zener diodes at the output of op-amp as shown in Fig. 2.11 (d).

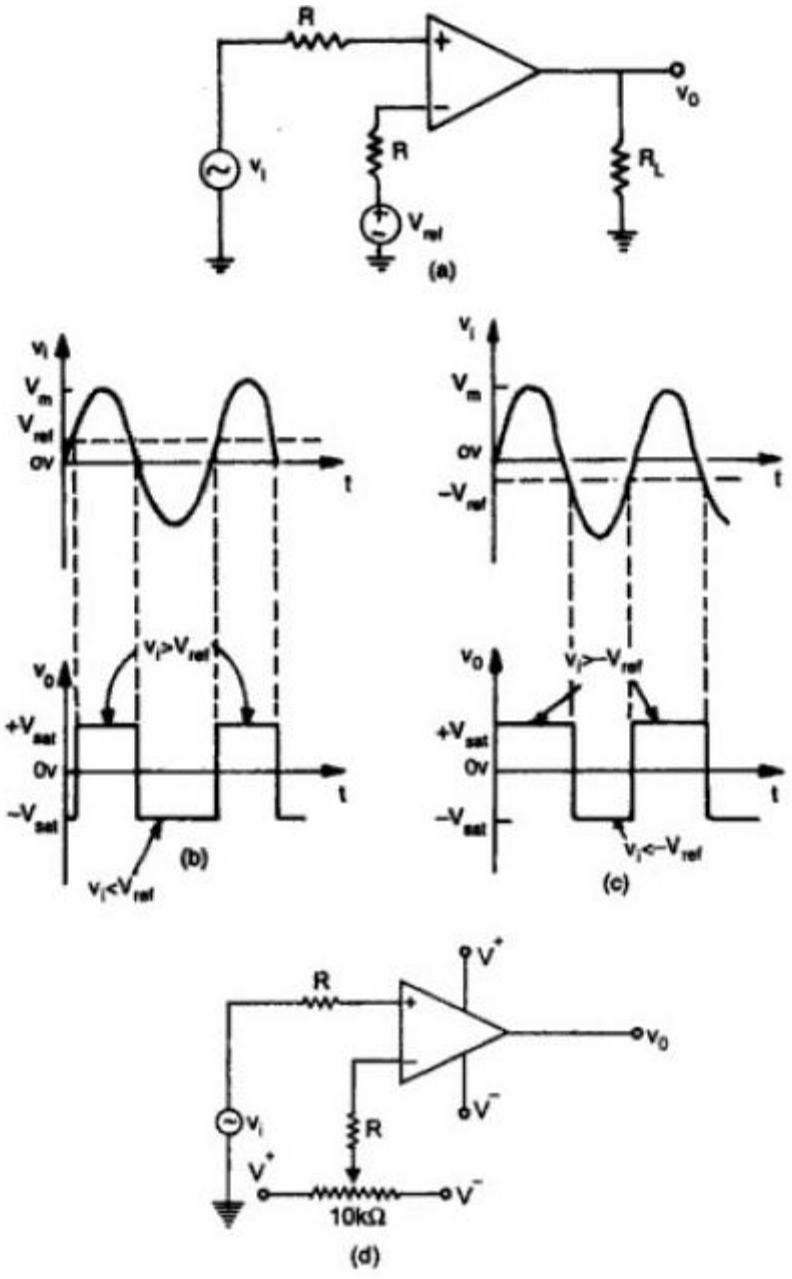


Figure 2.10

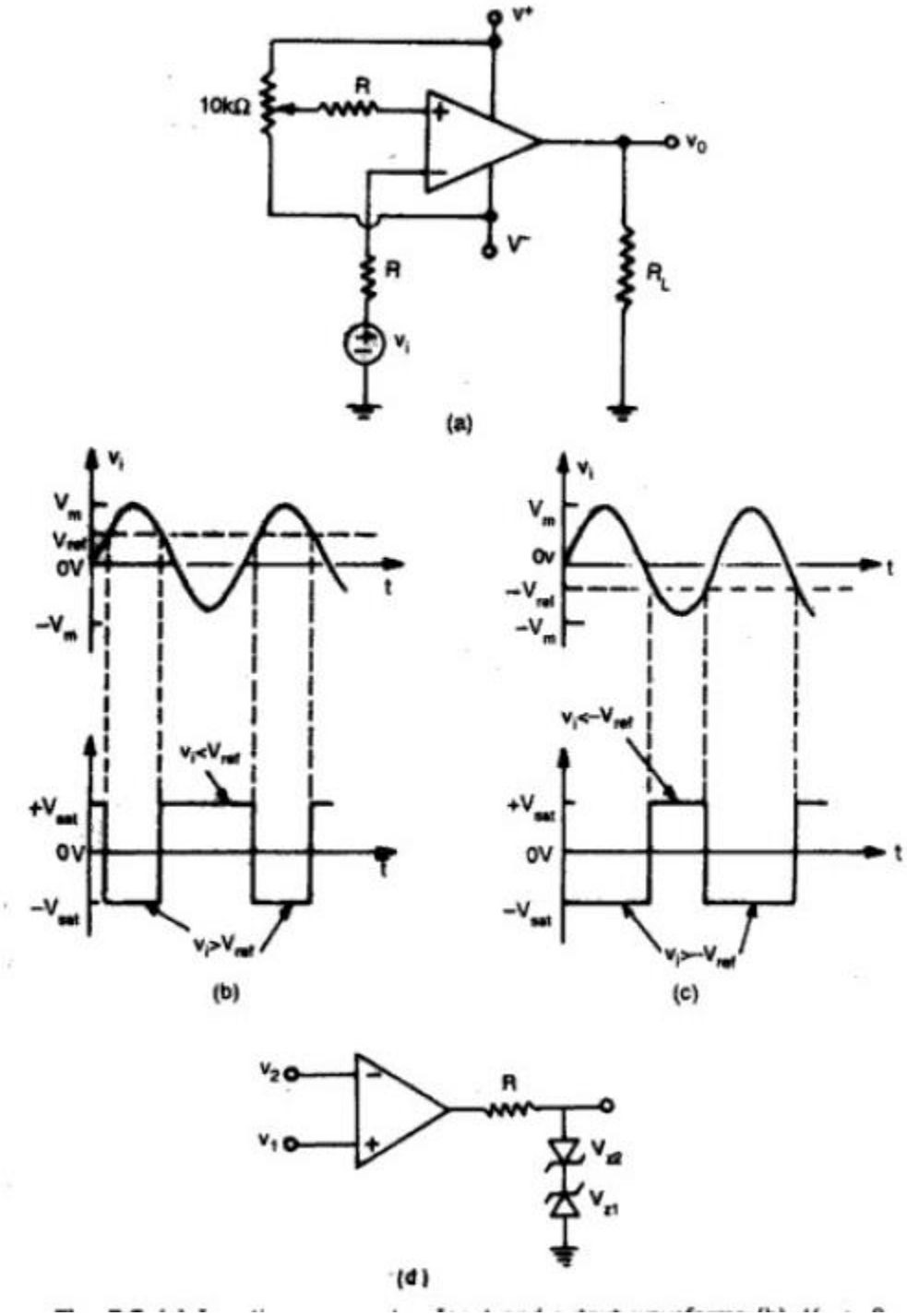

V+
10kΩ
R
Vo
V-
R
RL
Vi
(a)
Vi
Vm
Vref
0V
-Vm
t
Vi<Vref
+Vsat
0V
-Vsat
Vi>Vref
(b)
Vi
Vm
0v
-Vref
-Vm
t
Vi<-Vref
+Vsat
0V
-Vsat
Vi>-Vref
(c)
V2
V1
R
Vz2
Vz1
(d)

Figure 2.11

2.2.5 Schmitt Trigger

When positive feedback is added to the comparator circuit, gain can be increased greatly. Consequently, the transfer curve of comparator becomes more close to ideal curve. Theoretically, if the loop gain $-\beta_{AoL}$ is adjusted to unity, then the gain with feedback, A_v, becomes infinite. This results in an abrupt (zero rise time) transition between the extreme values of output voltage. In practical circuits, however, it may not be possible to maintain loop-gain exactly equal to unity for a long time because of supply voltage and temperature variations. So a value greater than unity is chosen. This also gives an output wave- form virtually discontinuous at the comparison voltage. This circuit, however, now exhibits a phenomenon called hysteresis or backlash.

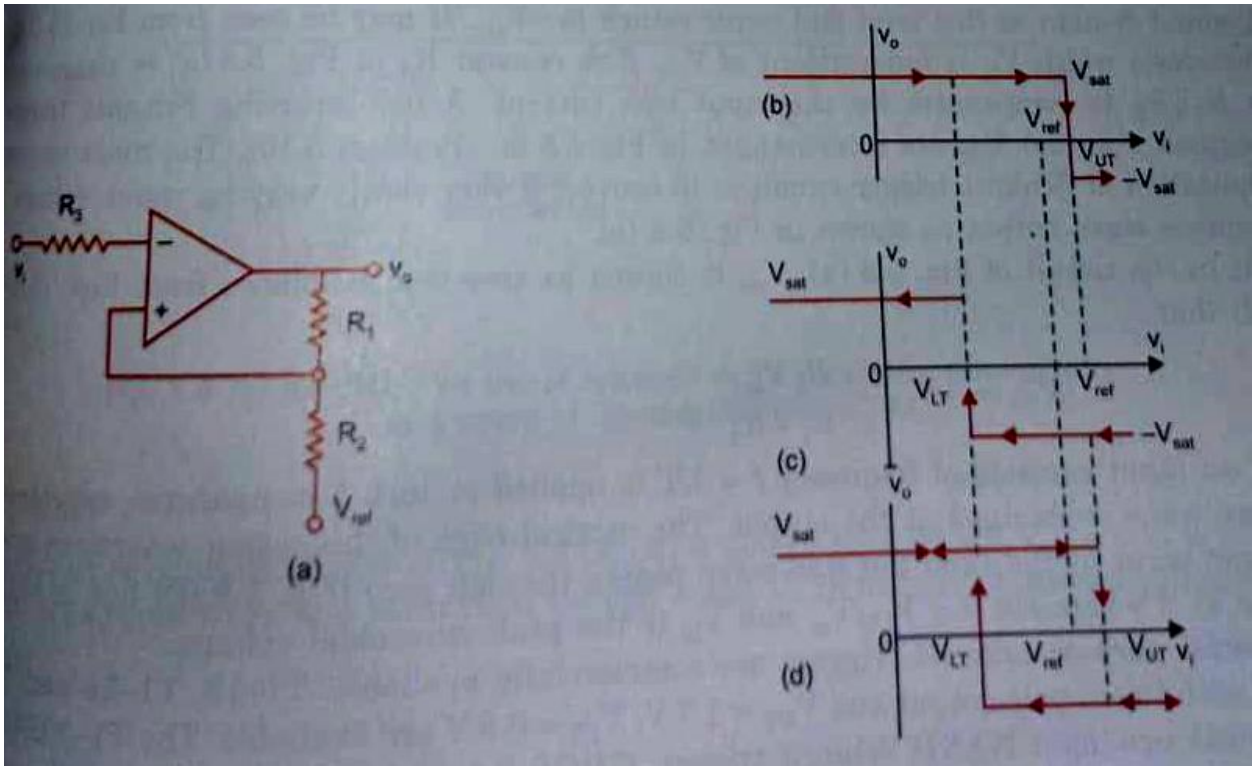


Figure 2.12

Figure 2.12 (a) shows such a regenerative comparator. The circuit is also known as Schmitt Trigger. The input voltage is applied to the (-) input terminal and feedback voltage to the (+) input terminal. The input voltage v triggers the output v, every time it exceeds certain voltage levels. These voltage levels are called upper threshold voltage (V_{UT}) and lower threshold voltage (V_{LT}). The hysteresis width is the difference between these two threshold voltages. These threshold voltages are calculated as follows.

$$V_{UT} = \frac{v_{ref}R_1}{R_1+R_2} + \frac{v_{sat}R_2}{R_1+R_2}$$

This voltage is called upper threshold voltage V_{UT}. As long as v_i is less than V_{UT}, the output V_o , remains constant at + Vsat. When v_i is just greater than V_{UT}, the output regeneratively switches to -Vsat and remains at this level as long as $v_i > V_{UT}$ as shown in Fig.2.12 (b). For v_o = -Vsat the voltage at the (+) input terminal is,

$$V_{LT} = \frac{v_{ref}R_1}{R_1+R_2} - \frac{v_{sat}R_2}{R_1+R_2}$$

This voltage is referred to as lower threshold voltage V_{LT} . The input voltage v_i must become lesser than V_{LT} in order to cause v_o, to switch from -Vsat to +Vsat. A regenerative transition takes place as shown in Fig.2.12 (c) and the output v_o returns from -Vsat to +Vsat almost instantaneously. The complete transfer characteristics are shown in Fig.2.12 (d).

Note that the difference between these two voltages is the hysteresis width V_H and can be written as

$$V_H = V_{UT} - V_{LT}$$

Figure 2.12(e) show the CRO output for the schmitt trigger

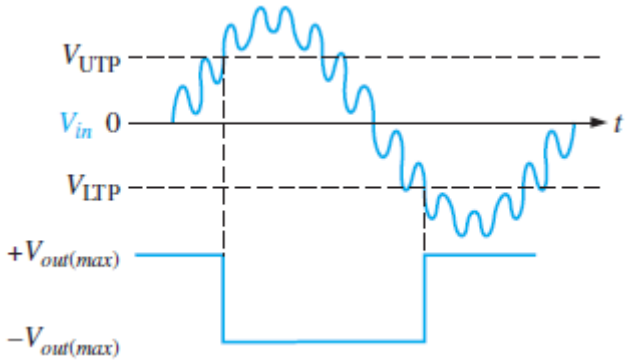


figure 2.12(e)

2.2.6 Multivibrators and Waveform generators

Astable Multivibrators [square wave generators]

A simple op-amp square wave generator is shown in Fig. 2.13 (a). Also called a free running oscillator, the principle of generation of square wave output is to force an op-amp to operate in the saturation region. In Fig.2.13 (a) fraction β = R2/(R1 + R2) of the output is fedback to the (+) input terminal. Thus the reference voltage Vref is v_o , and may take values $+\beta V_{sat}$ or $-\beta V_{sat}$.

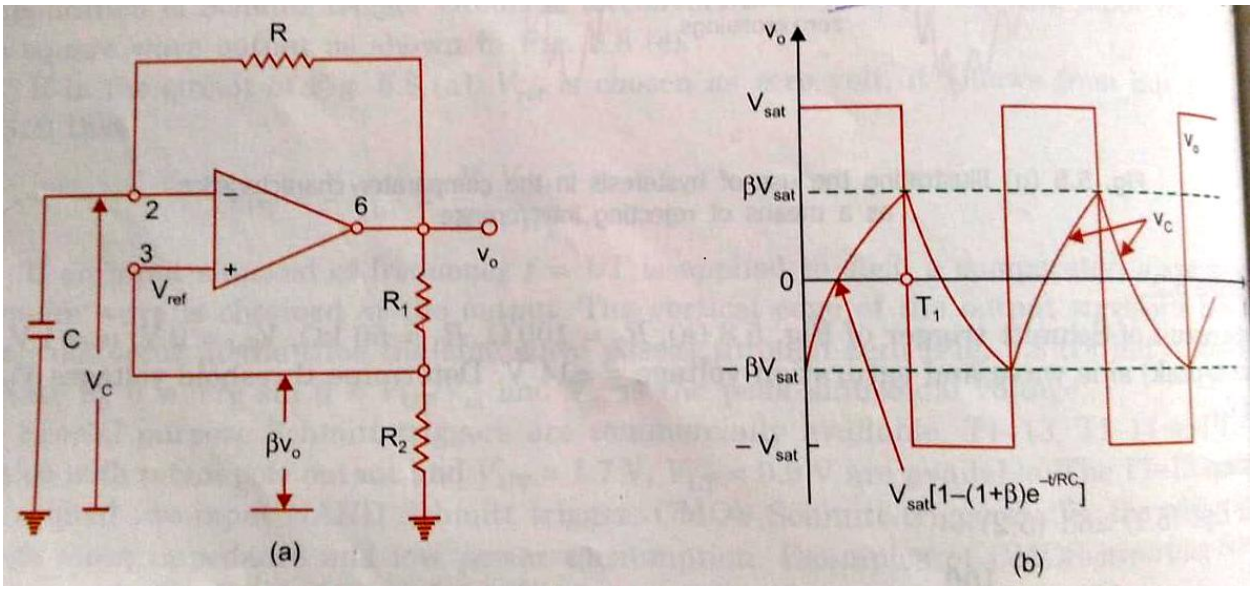


Figure 2.13

The output is also fed back to the (-) input terminal after integrating by means of a low-pass RC combination. Whenever input at the (-) input terminal just exceeds Vref switching takes place resulting in a square wave output. In astable multivibrator, both the states are quasi stable. The capacitor now starts charging

Consider an instant of time when the output is at +Vsat towards-Vsat through-resistance R, as shown in Fig. 2.13 (b). The voltage at the (+) input terminal is held at + βV_{sat} by R, and RC, combination. This condition continues as the charge on C rises, until it has just exceeded + βV_{sat} the reference voltage. When the voltage at the (-) input terminal becomes just greater than this reference voltage, the output is driven to At this instant, the voltage on the capacitor is + βV_{sat}. It begins to discharge through R. that is, charges toward –Vsat. When the output voltage switches to –Vsat the capacitor charges more and more negatively until its voltage just exceeds - βV_{sat} The output switches back to + V . The cycle repeats itself as shown in Fig.2.13 (b). The frequency is determined by the time it takes the capacitor to charge from - βV_{sat} to +Vsat and vice versa. The voltage across the capacitor as a function of time is given by,

$v(t) = Vf + (Vi-Vf)\exp(-t/RC)$

$V_f = +Vsat$

$V_i = -\beta V_{sat}$

When $t=T_1$,

$T_1 = RC \frac{1+\beta}{1-\beta}$

$T = 2\ T_1 = 2\ RC \frac{1+\beta}{1-\beta}$

When $\beta=1/2$,we get

$T = 2.2\ RC$

MONOSTABLE MULTIVIBRATOR

Monostable multivibrator has one stable state and the other is quasi stable state, the is useful for generating single output pulse of adjustable time duration in response to triggering signal.The width of the output pulse depends only on external components connected to the op-amp. The circuit shown in Fig. 2.14(a) is a modified form of the astable multivibrator. A diode D1 clamps the capacitor voltage to 0.7 V when the output is at +VA negative going pulse signal of magnitude V1 passing through the differentiator RC, and diode L produces a negative going triggering impulse and is applied to the (+) input terminal. To analyze the circuit, let us assume that in the stable state, the output Vo, is at +Vsat and diode D1 conducts and v, the voltage across the capacitor C gets clamped to +0.7 V. The voltage at the (+) input terminal through R_1 R_2 potentiometric divider is + β V_{sat} Now, negative trigger of magnitude V, is applied to the (+) input terminal so that the effective signal at this terminal is less than 0.7 V, i.e. ([β Vsat+(-V1)]< 0.7 V), the output of the op amp will switch from + V_{sat} to - V_{sat} .The diode will now get reverse biased and the capacitor starts charging exponentially to -Vsat through the resistance R..The voltage at the (+) input terminal is now - β V_{sat}. When the capacitor voltage v, becomes just slightly more negative the output of the op-amp switches back to + V_{sat}. The capacitor C now starts charging to + V_{sat} through R until v, is 0.7V as capacitor C gets clamped to the voltage .The pulse width T of monostable multivibrator is calculated as follows:

The general solution for a single time constant low pass RC circuit with V, and V, as initial and final values is,

$v(t) = Vf + (Vi-Vf)\exp(-t/RC)$

$Vf= -V\ sat$

$Vi= V_D$

At t=T

$T= RC \ln \frac{(1+Vd+V\ sat)}{1-\beta}$

When $\beta=\frac{R_1}{R_1+R_2}=0.5$

T= 0.69 RC

For monostable operation, the trigger pulse width should be much less than the T. pulse width of the monostable multivibrator. The diode D is used to avoid malfunctioning by blocking the positive noise spikes that may be present at the differentiated trigger input It may be noted from Fig. 2.14 (b) that capacitor voltage u, reaches its quiescent value V at T. Therefore, it is essential that a recovery time T.T be allowed to elapse before the next triggering signal is applied. The circuit of Fig. 2.14 (a) can be modified to achieve voltage to time delay conversion as in the case of square wave generators. The monostable multivibrator circuit is also referred to as time delay circuit as it generates a fast transition at a predetermined time T after the application of input trigger. It is also called a gating circuit as it generates a rectangular waveform at a definite time and thus could be used gate parts of a system.

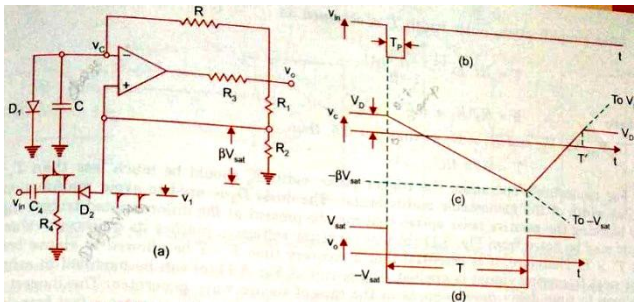


Figure 2.14

TRIANGULAR WAVE GENERATOR

A triangular wave can be simply obtained by integrating a square wave as shown in Fig 2.15 (a). It is obvious that the frequency of the square wave and triangular wave is the same as shown in Fig.2.15 (b). Although the amplitude of the square wave is constant at V the amplitude of the triangular wave will decrease as the frequency increases. This because the reactance of the capacitor C, in the feedback circuit decreases at high frequencies A resistance R, is connected across C, to avoid the saturation problem at low frequencies as in the case of practical integrator.

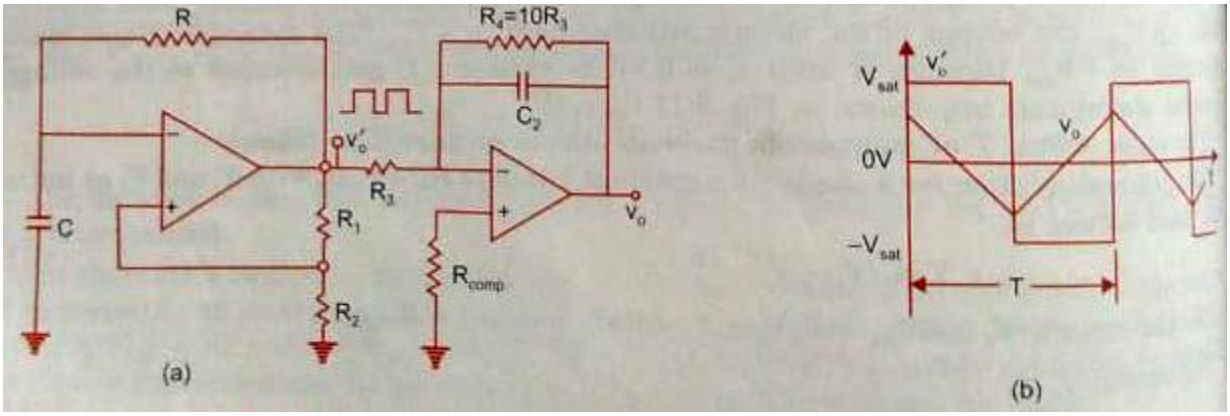


Figure 2.15

UNIT-III ACTIVE FILTERS,TIMERS AND PHASE LOCKED LOOPS

ACTIVE FILTERS: Introduction, Butterworth filters – 1st order, 2nd order low pass and high pass filters, band pass, band reject and all pass filters.

TIMER AND PHASE LOCKED LOOPS: Introduction to IC 555 timer, description of functional diagram, monostable and astable operations and applications, Schmitt trigger, PLL - introduction, basic principle, phase detector/comparator, voltage controlled oscillator (IC 566), low pass filter, monolithic PLL and applications of PLL

3.1 Active Filters

3.1.1 Introduction

Filters are circuits that are capable of passing signals with certain selected frequencies while rejecting signals with other frequencies. This property is called *selectivity*. Active filters use transistors or op-amps combined with passive *RC*, *RL*, or *RLC* circuits. The active devices provide voltage gain, and the passive circuits provide frequency selectivity. Although inductors are used in passive filters, they are avoided in active filters because inductors tend to be bulky, more expensive than capacitors, and not easily integrated. In terms of general response, the four basic categories of active filters are low-pass, high-pass, band-pass, and band-stop. In this chapter, you will study active filters using op-amps and *RC* circuits.

3.1.2 Butterworth Characteristics:

The **Butterworth** characteristic provides a very flat amplitude response in the passband and a roll-off rate of -20 dB/decade/pole. The phase response is not linear, however, and the phase shift (thus, time delay) of signals passing through the filter varies nonlinearly with frequency. Therefore, a pulse applied to a filter with a Butterworth response will cause overshoots on the output because each frequency component of the pulse's rising and falling edges experiences a different time delay. Filters with the Butterworth response are normally used when all frequencies in the pass band must have the same gain. The Butterworth response is often referred to as a maximally flat response.

3.1.3 Active low pass filters

1st Order low pass filter:

Figure 3.1(a) shows an active filter with a single low-pass *RC* frequency-selective circuit that provides a roll-off of -20 dB/decade above the critical frequency, as indicated by the response curve in Figure 3.1(b). The critical frequency of the single-pole filter is $f_c = 1/(2\pi RC)$.

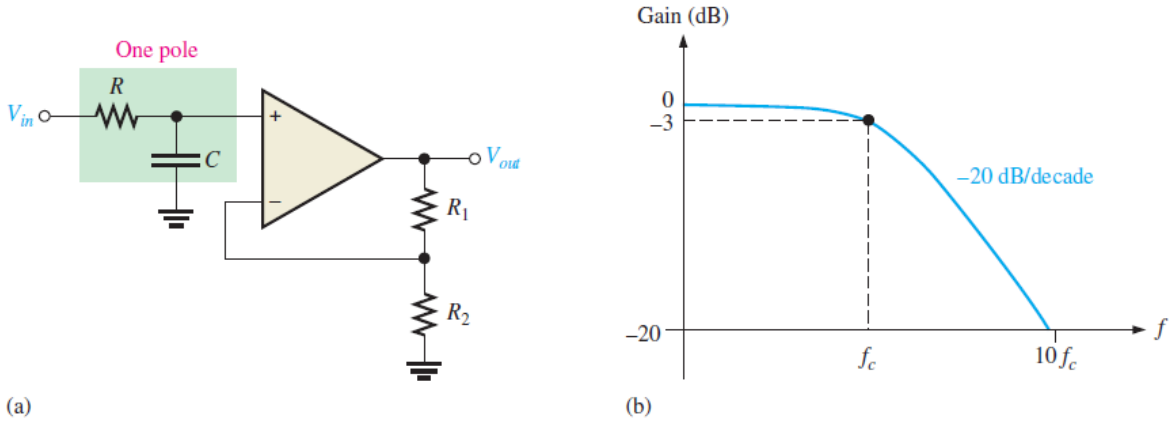


Figure 3.1

2nd Order low pass filter:

The Sallen-Key is one of the most common configurations for a second-order (two-pole) filter. It is also known as a VCVS (voltage-controlled voltage source) filter. A low-pass version of the Sallen-Key filter is shown in Figure 3.2. Notice that there are two lowpass *RC* circuits that provide a roll-off of -40 dB/decade above the critical frequency (assuming a Butterworth characteristic). One *RC* circuit consists of R_A and C_A, and the second circuit consists of R_B and C_B. A unique feature of the Sallen-Key low-pass filter is the capacitor *CA* that provides feedback for shaping the response near the edge of the pass band. The critical frequency for the Sallen-Key filter is

$$f_c \frac{1}{\sqrt{2\pi R_A R_B C_A C_B}}$$

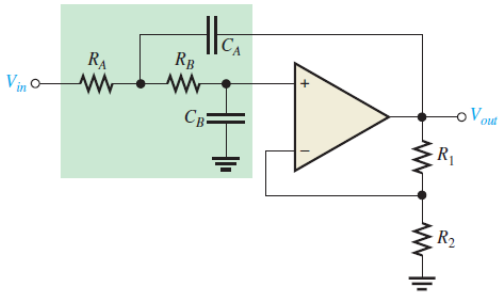
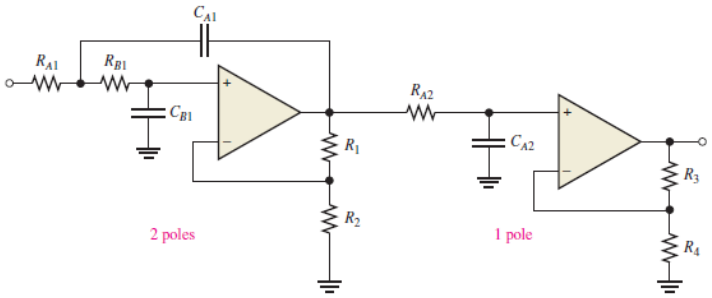


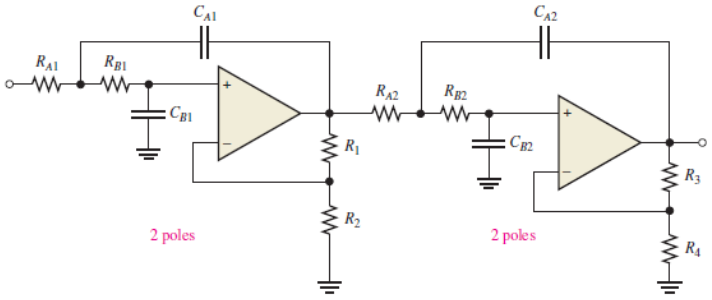
Figure 3.2

Higher order Low pass filters

A three-pole filter is required to get a third-order low-pass response (-60 dB/decade). This is done by cascading a two-pole Sallen-Key low-pass filter and a single-pole lowpass filter, as shown in Figure 3.3(a). Figure 3.3(b) shows a four-pole configuration obtained by cascading two Sallen-Key (two-pole) low-pass filters. In general, a four-pole filter is preferred because it uses the same number of op-amps to achieve a faster roll-off.



(a) Third-order configuration



(b) Fourth-order configuration

Figure 3.3

3.1.4 Active High pass filters

1st order High pass filter

A high-pass active filter with a -20 dB/decade roll-off is shown in Figure 3.4(a). Notice

that the input circuit is a single high-pass *RC* circuit. The negative feedback circuit is the same as for the low-pass filters previously discussed. The high-pass response curve is shown in Figure 3.4(b).

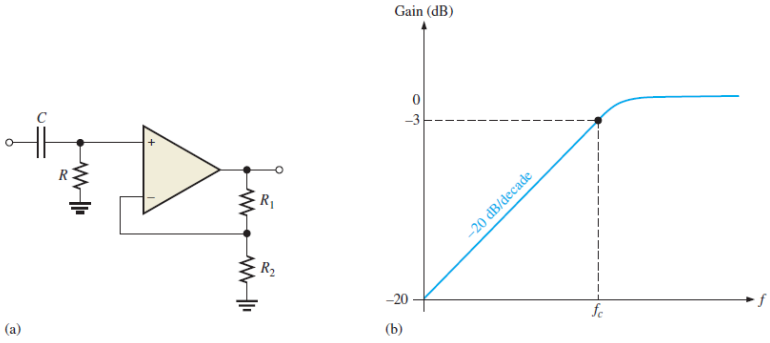


figure 3.5

2nd order High pass filter

A high-pass Sallen-Key configuration is shown in Figure 3.6. The components R_A, C_A, R_B, and C_B form the two-pole frequency-selective circuit. Notice that the positions of the resistors and capacitors in the frequency-selective circuit are opposite to those in the low-pass configuration. As with the other filters, the response characteristic can be optimized by proper selection of the feedback resistors, *R*1 and *R*2.

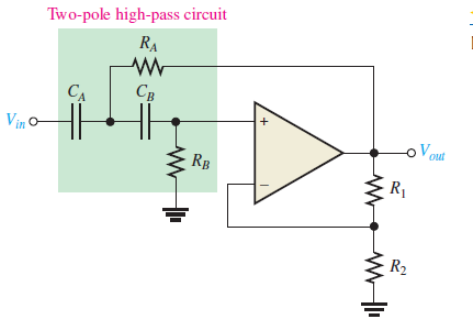


Figure 3.6

Higher order High pass Filter

As with the low-pass configuration, first- and second-order high-pass filters can be cascaded to provide three or more poles and thereby create faster roll-off rates. Figure 3.7 shows a six-pole high-pass filter consisting of three Sallen-Key two-pole stages. With this configuration optimized for a Butterworth response, a roll-off of -120 dB/decade is achieved.

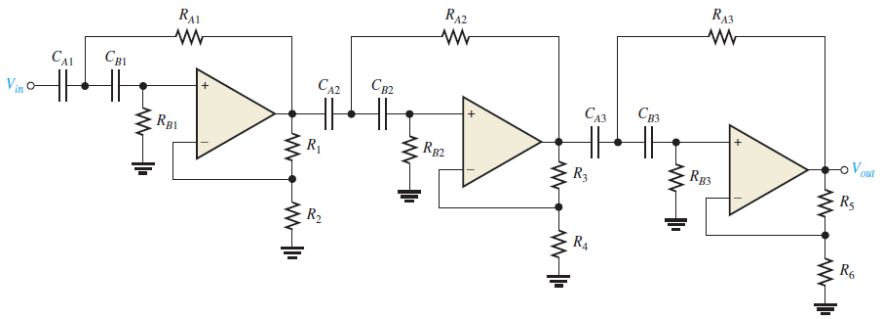


Figure 3.7

3.1.5 Active Band pass filter

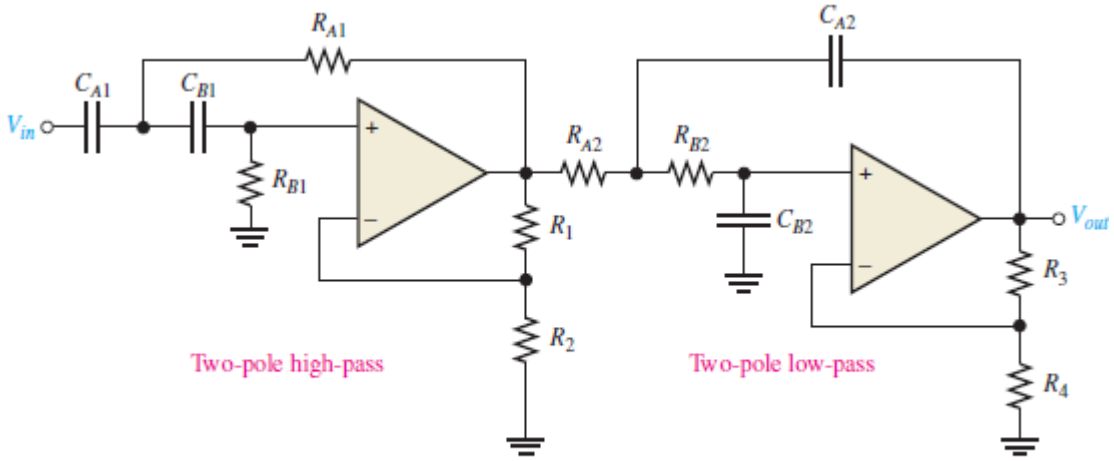
Cascading of High Pass and Low Pass Filters

One way to implement a band-pass filter is a cascaded arrangement of a high-pass filter and a low-pass filter, as shown in Figure 3.8(a), as long as the critical frequencies are sufficiently separated. Each of the filters shown is a Sallen-Key Butterworth configuration so that the roll-off rates are -40 dB/decade, indicated in the composite response curve of Figure 3.8(b). The critical frequency of each filter is chosen so that the response curves overlap sufficiently, as indicated. The critical frequency of the high-pass filter must be sufficiently lower than that of the low-pass stage. This filter is generally limited to wide bandwidth applications. The lower frequency *fc*1 of the passband is the critical frequency of the high-pass filter. The upper frequency *fc*2 is the critical frequency of the low-pass filter. Ideally, as discussed earlier, the center frequency *f*0 of the passband is the geometric mean of *fc*1 and *fc*2.

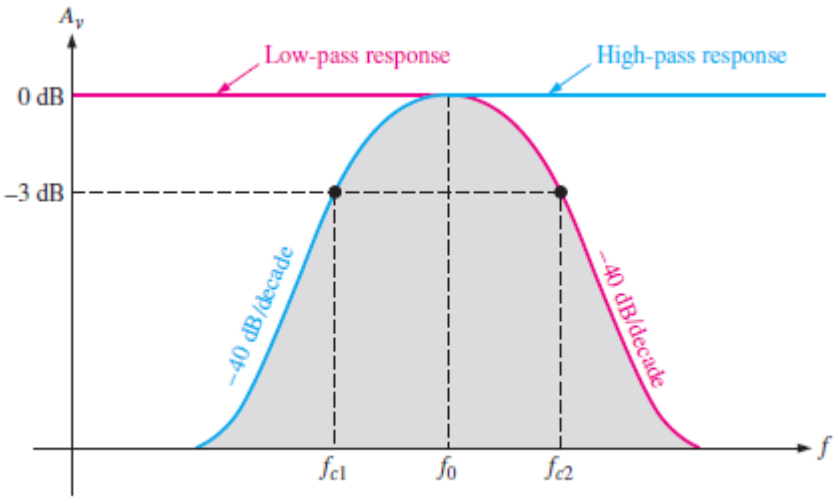
$$f_{c1} = \frac{1}{\sqrt{2\pi R_A R_B C_A C_B}}$$

$$f_{c2} = \frac{1}{\sqrt{2\pi R_A R_B C_A C_B}}$$

$$f_0 = \sqrt{fc1 fc2}$$



(a)



(b)

Figure 3.8

3.1.6 Band Stop Filter

Multiple Feedback Band Stop filter

Another category of active filter is the **band-stop filter**, shown in Figure 3.9 also known as *notch*, *band-reject*, or *band-elimination* filter. You can think of the operation as opposite to that of the bandpass filter because frequencies within a certain bandwidth are rejected, and frequencies outside the bandwidth are passed. A general response curve for a band-

stop filter is shown in Figure3.10. Notice that the bandwidth is the band of frequencies between the 3 dB points, just as in the case of the band-pass filter response.

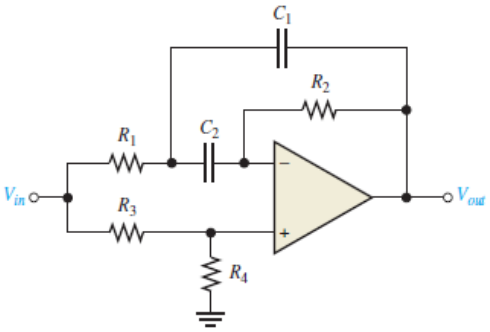


Figure 3.9

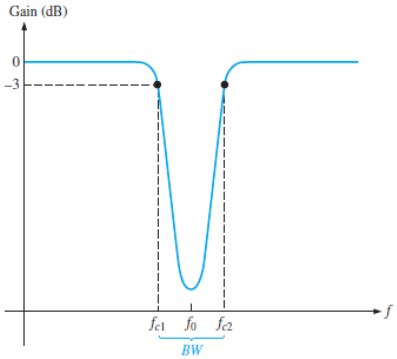


Figure 3.10

3.2 Timers

3.2.1 Introduction to IC 555 timer

The 555 timer is a highly stable device for generating accurate time delay or oscillation, Signetics Corporation first introduced this device as the SE555/NE555 and it is available in two package styles, 8-pin circular style, TO-99 can or 8-pin mini DIP or as 14-pin DIP. The 556 timer contains two 555 timers and is a 14-pin DIP. There is also available counter timer such as Exar's XR-2240 which contains a 555 timer plus a programmable binary counter in a single 16-pin package A single 555 timer can provide time delay ranging from microseconds to hours whereas counter timer can have a maximum timing range of days.

The 555 timer can be used with supply voltage in the range of +5V to + 18V and can drive load upto 200 mA. It is compatible with both TTL and CMOS 7 logic circuits. Because of the wide range of supply voltage, the 555 timer is versatile and easy to use in various applications. Various applications include oscillator, pulse generator, ramp and square wave generator, mono-shot multivibrator, burglar, alarm, traffic light control and voltage monitor etc.

3.2.2 DESCRIPTION OF FUNCTIONAL DIAGRAM

Figure3.11 gives the pin diagram and Fig. 3.12 gives the functional diagram for 555 IC timer. Referring to Fig.3.11, three 5 kΩ internal resistors act as voltage divider, providing bias voltage of (2/3) Vcc to the upper comparator (UC) and (1/3) Vcc to the lower comparator (LC), where Vec is the supply voltage. Since these two voltages fix the necessary comparator threshold voltage, they also aid in determining the timing interval. It is possible to vary time electronically too, by applying a modulation voltage to the control voltage input terminal (pin 5). In applications, where no such modulation is intended, it is recommended by manufacturers that a capacitor (0.01 μF) be connected between control voltage terminal (pin 5) and ground to by-pass noise or ripple from the supply.

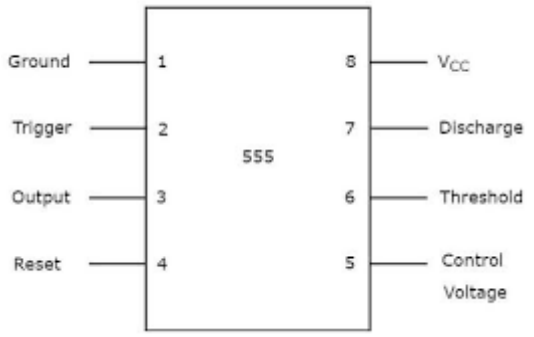


Figure 3.11

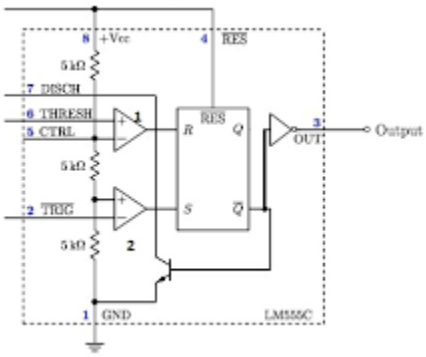


Figure 3.12

In the standby (stable) state, the output $\underline{Q}$ of the control flip-flop (FF) is HIGH. This makes the output LOW because of the power amplifier which is basically an inverter. A negative going trigger pulse is applied to pin 2 and should have its dc level greater than the threshold level of the lower comparator (i.e. Vcc/3). At the negative going edge of the trigger, as the trigger passes through (Vcc/3), the output of the lower comparator goes HIGH and sets the FF (Q= 1, $\underline{Q}$= 0). During the positive excursion, when the threshold voltage at pin 6 passes through (2/3) Vcc, the output of the upper comparator goes HIGH and resets the FF ($\underline{Q}$= 1, Q = 0). The reset input (pin 4) provides a mechanism to reset the FF in a manner which overrides the effect of any instruction coming to FF from the lower comparator. This overriding reset is effective when the reset input is less than about 0.4 V. When this reset is not used, it is returned to Vcc. The transistor Q2 serves as a buffer to isolate the reset input from the FF and transistor Q1. The transistor Q2 is driven by an internal reference voltage Vref obtained from supply voltage Vcc.

3.2.3 Monostable Operation

Figure 3.13 shows a 555 timer connected for monostable operation and its functional diagram is shown in Fig.3.14. In the standby state, FF holds transistor Q, on, thus clamping the external timing capacitor C to ground. The output remains at ground potential, i.e. LOW. As the trigger passes through Vcc/3, the FF is set, i.e. $\underline{Q}$ = 0. This makes the transistor Q1 off and the short circuit across the timing capacitor C is released. As Q1 is LOW, output goes HIGH (= Vcc). The timing cycle now begins. Since C is unclamped, voltage across it rises exponentially through R towards Vcc with a time constant RC as in Fig.3.15(b). After a time period T (calculated later), the capacitor voltage is just greater than (2/3) Vcc and the upper comparator resets the FF, that is, R = 1, S = 0 (assuming very small trigger pulse width). This makes Q = 1, transistor Q1 goes on (i.e. saturates), thereby discharging the capacitor C rapidly to ground potential. The output returns to the standby state or ground potential as shown in Fig. 3.15 (c).

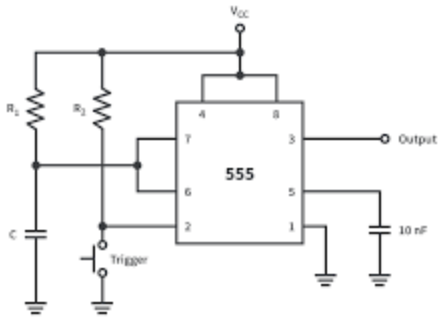


Figure 3.13

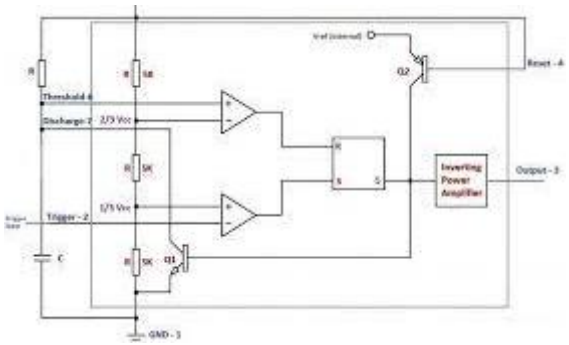


Figure 3.14

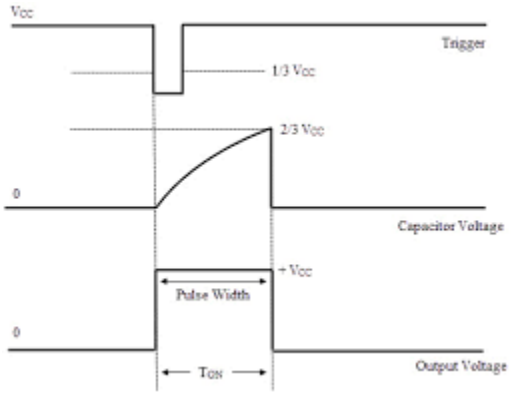
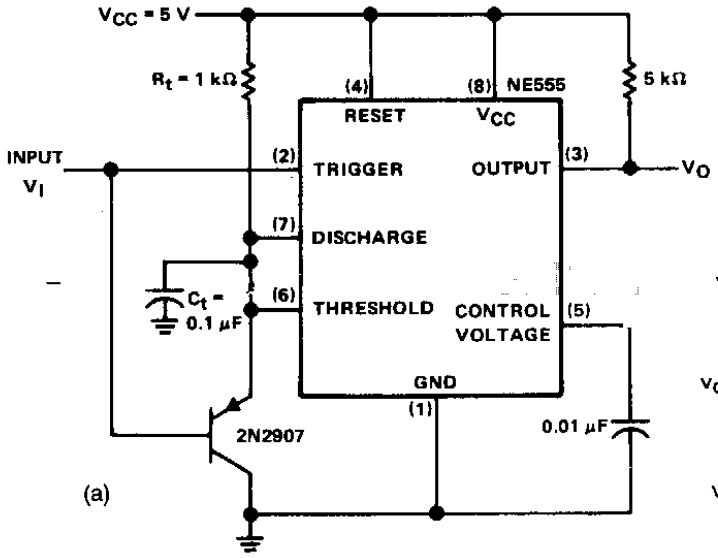


Figure 3.15

Applications of Monostable Operations

Missing Pulse Detector



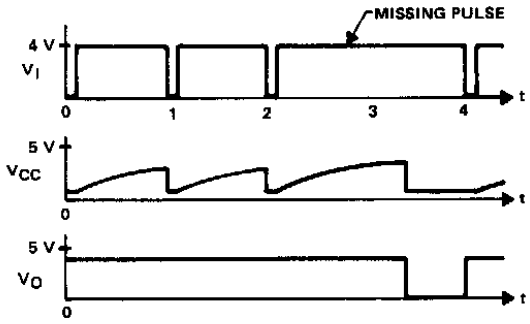


Figure 3.16 (a)

Figure 3.16(b)

Missing pulse detector circuit using 555 timer is shown in Fig.3.16(a). Whenever, input trigger is low, the emitter diode of the transistor Q is forward biased. The capacitor C gets clamped to few tenths of a volt (~ 0.7 V). The output of the timer goes HIGH. The circuit is designed so that the time period of the monostable circuit is slightly greater (1/3 longer) than that of the triggering pulses. So long the trigger pulse train keeps coming at pin 2, the output remains HIGH. However, if a pulse misses, the trigger input is high and transistor Q is cutoff. The 555 timer enters into normal state of monostable operation. The output goes LOW after time T of the mono-shot. Thus this type of circuit can be used to detect missing heartbeat. It can also be used for speed control and measurement. If input trigger pulses are generated from a rotating wheel, the circuit tells when the wheel speed drops below a predetermined value.

Frequency Divider

A continuously triggered monostable circuit when triggered by a square wave generator can be used as a frequency divider, if the timing interval is adjusted to be longer than the period of the triggering square wave input signal. The monostable multivibrator will be triggered by the first negative going edge of the square wave input but the output will remain HIGH (because of greater timing interval) for next negative going edge of the input square wave as shown in Fig.3.17. The mono-shot will however be triggered on the third negative going input, depending on the choice of the time delay. In this way, the output can be made integral fractions of the frequency of the input triggering square wave.

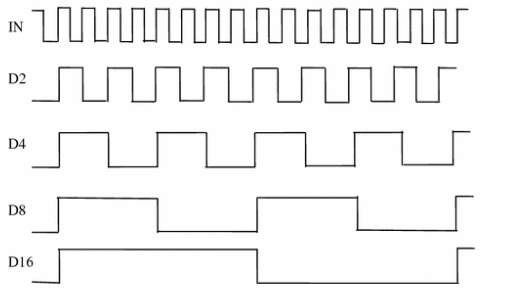


Figure 3.17

Pulse Width Modulation

The circuit is shown in Fig.3.18. This is basically a monostable multivibrator with a modulating input signal applied at pin-5. By the application of a continuous trigger at pin-2, a series of output pulses are obtained. the duration of which depends on the modulating input at pin-5. The modulating signal applied at pin-5 gets superimposed upon the already existing voltage (2/3) Vec the inverting input terminal of UC. This in turn changes the threshold level of UC and the output pulse width modulation takes place. The modulating signal and the output waveform are shown in Fig. 3.18. It may be noted from the output waveform that the pulse duration, that is, the duty cycle only varies, keeping the frequency same as that of the continuous input pulse at train trigger.

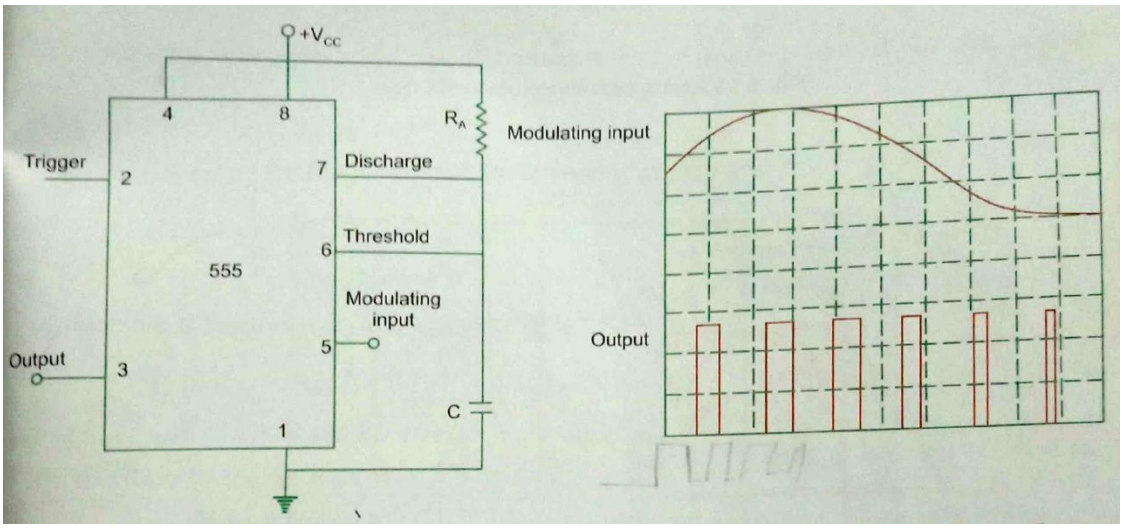


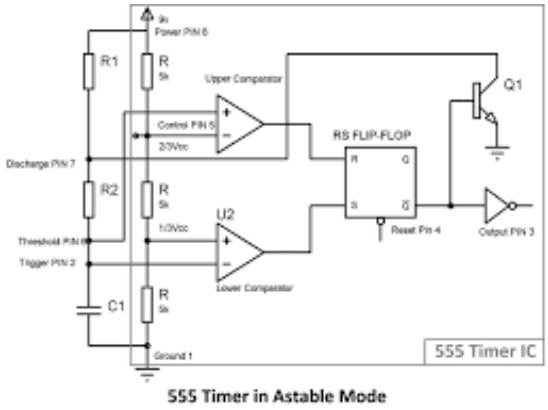
Figure 3.18

3.2.4 Astable Operation

The device is connected for astable operation as shown in Fig.3.19. For better understanding, the complete diagram of astable multivibrator with a detailed internal diagram of 555 is shown in Fig.3.19. Compared with monostable operation, the timing resistor is now split into two sections R and RB. Pin 7 of discharging transistor Q, is connected to the junction of R_A and R_B. When the power supply Vcc is connected, the external timing capacitor C charges towards Vcc with a time constant $(R_A + R_B)C$. During this time, output (pin 3) is high (equals Vcc) as Reset R = 0, Set S = 1 and this combination makes $\underline{Q}$ = 0 which has unclamped the timing capacitor C.

When the capacitor voltage equals (to be precise is just greater than), (2/3) Vcc the upper comparator triggers the control flip-flop so that $\underline{Q}$=1. This, in turn, makes transistor Q, on and capacitor C starts discharging towards ground through R_B and transistor Q, with a time constant R_BC(neglecting the forward resistance of Q1). Current also flows into transistor Q through R. Resistors R_A and R_B must be large enough to limit this current and prevent damage to the discharge transistor Q1. The minimum value of R_A is approximately equal to Vcc/0.2 where 0.2 A is the maximum current through the on transistor Q. During the discharge of the timing capacitor C, as it reaches (to be precise, is just less than) Vcc/3, the lower comparator is triggered

and at this stage S = 1, R = 0, which turns $\underline{Q}$= 0. Now $\underline{Q}$ = 0 unclamps the external timing capacitor C. The capacitor C is thus periodically charged and discharged between (2/3) Vcc and (1/3) Vcc respectively. Figure 3.20 shows the timing sequence and capacitor voltage wave form. The length of time that the output remains HIGH is the time for the capacitor to charge from (1/3) Vcc to (2/3) Vcc.



555 Timer in Astable Mode

Figure 3.19(a)

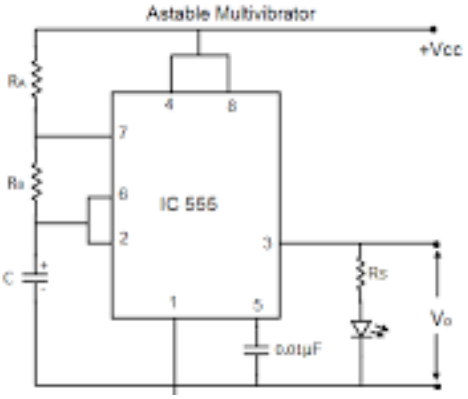


Figure 3.19(b)

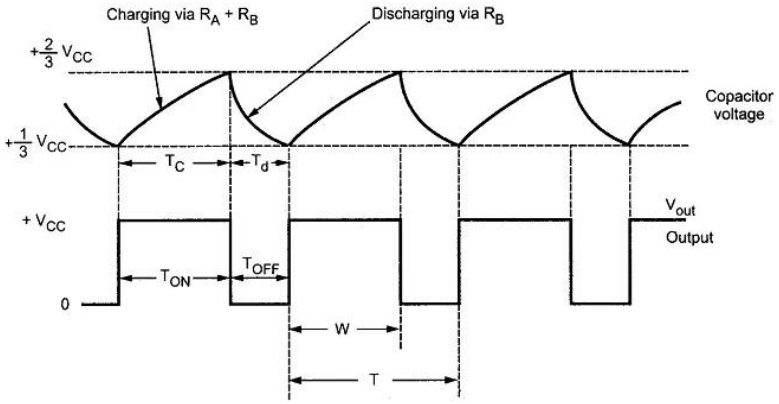


Figure 3.20

Applications of Astable Operation

Frequency Shift Keying Generator

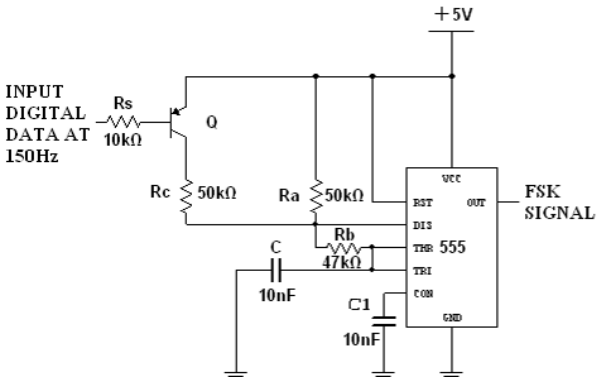


figure 3.21

In digital data communication, binary code is transmitted by shifting a carrier frequency between two preset frequencies. This type of transmission is called frequency shift keying (FSK) technique. A 555 timer in astable mode can be used to generate FSK signal. The circuit is as shown in Fig.3.21. The standard digital data input frequency is 150 Hz. When input is HIGH, transistor Q is off and 555 timer works in the normal astable mode of operation. The frequency of the output waveform given by Eq. (9.1) can be rewritten as

$f_o = 1.45/(R_A + 2R_B)C$

In a tele-typewriter using a modulator-demodulator (MODEM), a frequency between 1070 Hz to 1270 Hz is used as one of the standard FSK signals. The components R_A and R_B and the capacitor C can be selected so that f_o is 1070 Hz. When the input is LOW, Q goes on and connects the resistance R_C across R_A. The output frequency is now given by

$f_o=1.45/(R_A||R_C) + 2R_B$

The resistance R_C can be adjusted to get an output frequency 1270 Hz.

Pulse Position Modulator

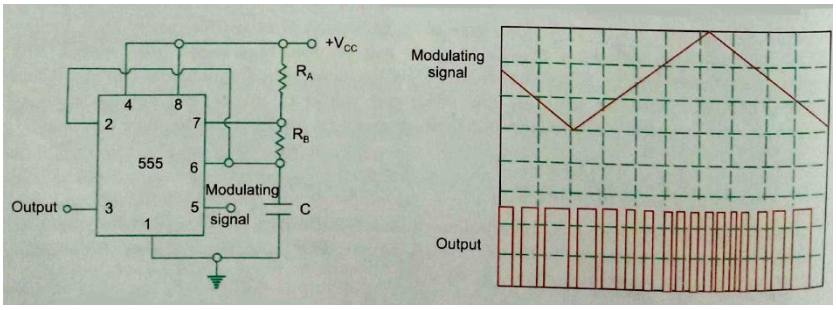


Figure 3.22

The pulse-position modulator can be constructed by applying a modulating signal to pin 5 of a 555 timer connected for astable operation as shown in Fig. 3.22. The output pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. Figure 9.23 shows the output waveform generated for a triangle wave modulation signal. It may be noted from the output waveform that the frequency is varying leading to pulse position modulation. The typical practical component values may be noted as

$R_A = 3.9\ k\Omega$, $R_B = 3\ k\Omega$, $C = 0.01\ \mu F$

Vcc = 5 V (any value between 5 V to 18 V may be chosen)

3.2.4 Schmitt Trigger

The use of 555 timer as a Schmitt Trigger is shown in Fig. 3.23. Here the two internal comparators are tied together and externally biased at Vcc/2 through R1 and R2. Since the upper comparator will trip at (2/3) Vcc and lower comparator at (1/3) Vcc, the bias provided by R1 and R2 is centered within these two thresholds. Thus, a sine wave of sufficient amplitude (> Vcc/6 = 2/3 Vcc - Vcc/2) to exceed the reference levels causes the internal flip-flop to alternately set and reset, providing a square wave output as shown in Fig. 3.24.

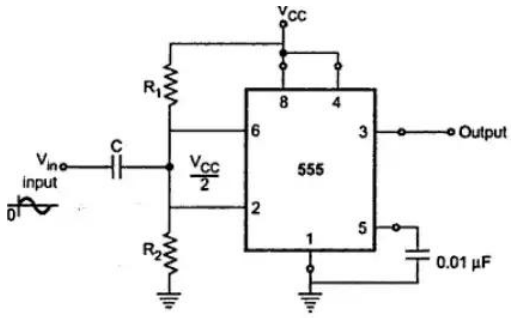


Figure 3.23

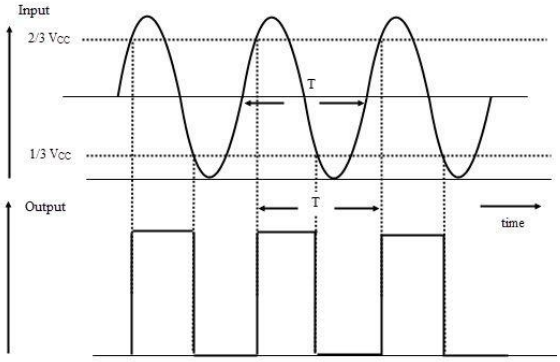


Figure 3.24

3.3 Phase Locked Loops

3.3.1 Introduction

The phase-locked loop (PLL) is an important building block of linear systems. Electronic phase-locked loop (PLL) came into vogue in the 1930s when it was used for radar synchronisation and communication applications. The high cost of realising PLL in discrete form limited its use earlier. Now with the advanced IC technology, PLLs are available as inexpensive monolithic ICs. This technique for electronic frequency control is used today in satellite communication systems, air borne navigational systems, FM communication systems, computers etc. The basic principle of PLL, different ICs and important applications are discussed.

3.3.2 Basic Principles Of PLL

The basic block schematic of the PLL is shown in Fig.3.25. This feedback system consists of:

1. Phase detector/comparator

2. A low pass filter

3. An error amplifier

4. A Voltage Controlled Oscillator (VCO)

The VCO is a free running multivibrator and operates at a set frequency f_0 called free running frequency. This frequency is deter- mined by an external timing capacitor and an external resistor. It can also be shifted to either side by applying a de control voltage v, to an appropriate terminal of the IC. The frequency deviation is directly proportional to the de control voltage and hence it is called a "Voltage Controlled Oscillator" or, in short, VCO.

If an input signal v_s of frequency f_s is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output v_o of the VCO. If the two signals differ in frequency and/or phase, an error voltage v_e is generated. The phase detector is basically a multiplier and produces the sum (f_s+f_o) and difference (f_s-f_o)components at its output. The high frequency component (f_s+f_o) is removed by the low pass filter and the difference frequency component is amplified and then applied as control voltage v to VCO. The signal v, shifts the VCO frequency in a direction to reduce the frequency difference between f, and fo. Once this action starts, we say that the signal is in the capture range. The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency. The circuit is then said to be locked. Once locked, the output frequency f, of VCO is identical to f, except for a finite phase difference . This phase difference generates a corrective control voltage v, to shift the VCO frequency from f, to f, and thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal. Thus, a PLL goes through three stages (i) free running, (ii) capture and (iii) locked or tracking.

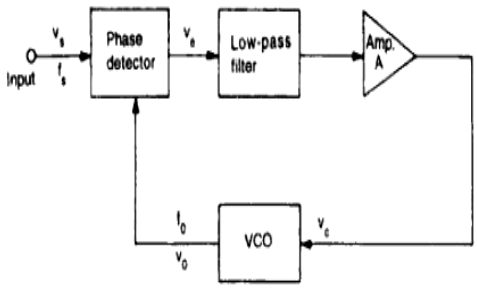


Figure 3.25

Figure 3.26 shows the capture transient. As capture starts, a small sine wave appears. This is due to the difference frequency between the VCO and the input signal. The de component of the beat drives the VCO towards the lock. Each successive cycle causes the VCO frequency to move closer to the input signal frequency. The difference in frequency becomes smaller and a large component is passed by the filter, shifting the VCO frequency further. The process continues until the VCO locks on to the signal and the difference frequency is dc.

The low pass filter controls the capture range. If VCO frequency is far away, the beat frequency will be too high to pass through the filter and the PLL will not respond. We say that the signal is out of the capture band. However, once locked, the filter no longer restricts the PLL. The VCO can track the signal well beyond the capture band. Thus tracking range is always larger than the capture range.

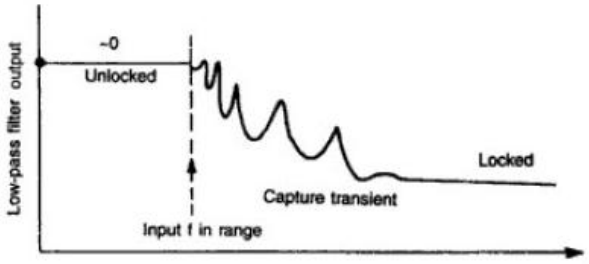


Figure 3.26

Some of the important definitions in relation to PLL are:

Lock-in Range: Once the PLL is locked, it can track frequency changes in the incoming signals. The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock- in range or tracking range. The lock range is usually expressed as a percentage of f_o, the VCO frequency.

Capture Range: The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of f_o

Pull-in time: The total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

3.3.3 Phase Detector/Comparator

The phase detection is the most important part of the PLL system. There are two types of phase detectors used, analog and digital.

Analog Phase Detector

The principle of analog phase detection using switch type phase detector is shown in Fig. 3.27(a). An electronic switch S is opened and closed by signal coming from VCO (normally a square wave) as shown in Fig. 3.27(b). The input signal is, therefore, chopped at a repetition rate determined by VCO frequency. Figure 3.27(c) shows the input signal v, assumed to be in phase (= 0°) with VCO output v. Since the switch S is closed only when VCO output is positive, the output waveform v will be half sinusoids (shown hatched). Similarly, the output waveform for = 90° and 180° is shown in Fig. 3.27(d, e). This type of phase detector is called a half wave detector, since the phase information for only one-half of the input waveform is detected and averaged. The output of the phase comparator when filtered through a low pass filter gives an error signal which is the average value of the output waveform shown by dotted line in Fig.

3.27(c, d, e). It may be seen that the error voltage is zero when the phase shift between the two inputs is 90°. So, for perfect lock, the VCO output should be 90° out of phase with respect to the input signal.

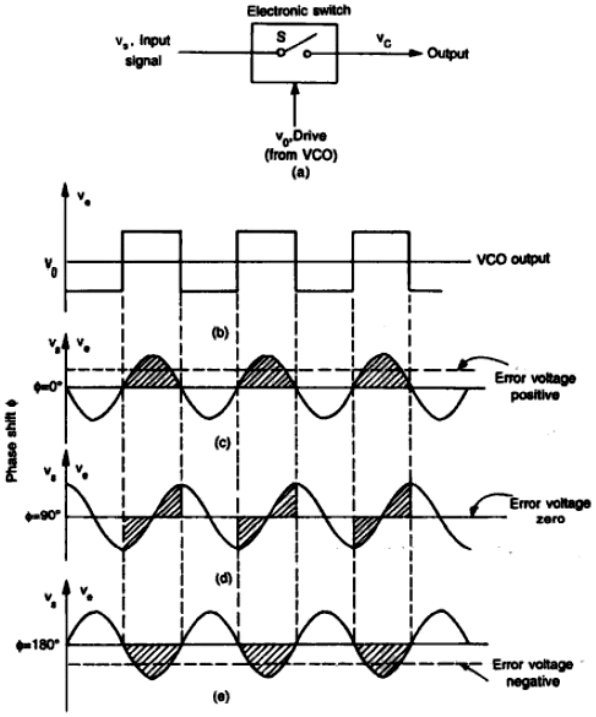


Figure 3.27

Digital Phase Detector

Figure 3.28(a) shows the digital type XOR (Exclusive-OR) phase detector. It uses CMOS type 4070 Quad 2-input XOR gate. The output of the XOR gate is high when only one of the inputs signals f_s or f_o is high. This type of detector is used when both the input signals are square waves. The input and output waveforms for $f_s = f_o$. are shown in Fig. 3.28(b). In this figure, f_s is leading f_o by φ degrees. The variation of dc output voltage with phase difference φ is shown in Fig. 3.28(c). It can be seen that the maximum de output voltage occurs when the phase difference π is a because the output of the gate remains high throughout. The slope of the curve gives the conversion ratio k_φ of the phase detector. So, the conversion ratio K_φ for a supply voltage Vcc = 5V is,

$K_\varphi = \frac{5}{\pi} = 1.59$ V/rad

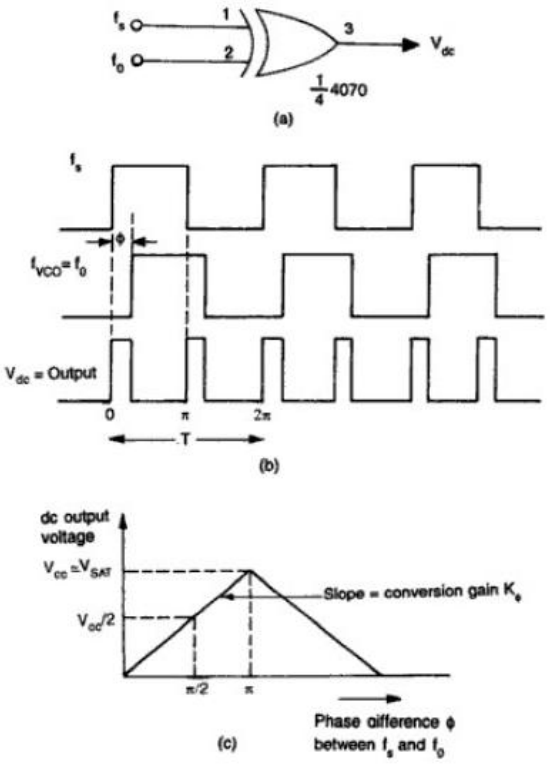


Figure 3.28

3.3.4 Voltage Controlled Oscillator

A common type of VCO available in IC form is Signetics NE/SE566. The pin configuration and basic block diagram of 566 VCO are shown in Fig.3.29(a, b). Referring to Fig. 3.29(b), a timing capacitor C_T is linearly charged or discharged by a constant current source/sink. The amount of current can be controlled by changing the voltage v_c applied at the modulating input (pin 5) or by changing the timing resistor R_T external to the IC chip. The voltage at pin 6 is held at the same voltage as pin 5. Thus, if the modulating voltage at pin 5 is increased, the voltage at pin 6 also increases, resulting in less voltage across R_T and thereby decreasing the charging current.

The voltage across the capacitor C_T is applied to the inverting input terminal of Schmitt trigger A_1 via buffer amplifier A_2. The output voltage swing of the Schmitt trigger is designed to Vcc

and 0.5 V If R_a=R_b in the positive feedback loop, the voltage at the non-inverting input terminal of A, swings from 0.5 V to 0.25 Vee In Fig. 3.29(c). when the voltage on the capacitor C_T exceeds 0.5 Vcc during charging, the output of the Schmitt trigger goes LOW (0.5 Vcc). The capacitor now discharges and when it is at 0.25 Vcc, the output of Schmitt trigger goes HIGH (Vcc). Since the source and sink currents are equal, capacitor charges and discharges for the same amount of time. This gives a triangular voltage waveform across C_T which is also available at pin 4. The square wave output of the Schmitt trigger is inverted by inverter A_3 and is available at pin 3. The output waveforms are shown in Fig. 3.29(c).

$$f_o = \frac{2(V_{cc}-V_c)}{R_T C_T V_{cc}}$$

if v_c = 7/8Vcc,then f_o ,

$$f_o = \frac{2(V_{cc}-7/8V_{cc})}{R_T C_T V_{cc}}$$

$$f_o = \frac{1}{4R_T C_T}$$

$$f_o = \frac{0.25}{R_T C_T}$$

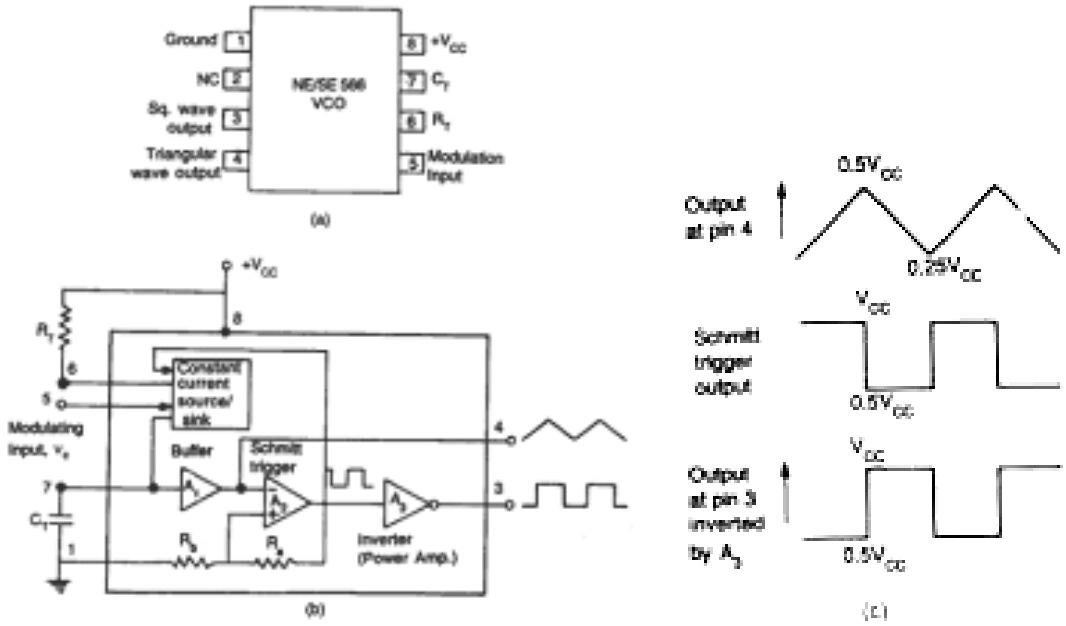


Figure 3.29

3.3.5 Low Pass Filter

The filter used in a PLL may be either passive type as shown in Fig. 3.30(a, b) or active type as in Fig. 3.30(c). The low pass filter not only removes the high frequency components and noise, but also controls the dynamic characteristics of the PLL. These characteristics include capture and lock range, band-width and transient response. If filter band-width is reduced, the response time increases. However, reducing the band-width of the filter also reduces the capture range of the PLL. The filter serves one more important purpose. The charge on the filter capacitor gives a short time 'memory' to the PLL. Thus, even if the signal becomes less than the noise for a few cycles, the dc voltage on the capacitor continues to shift the frequency of the VCO till it picks up signal again. This produces a high noise immunity and locking stability.

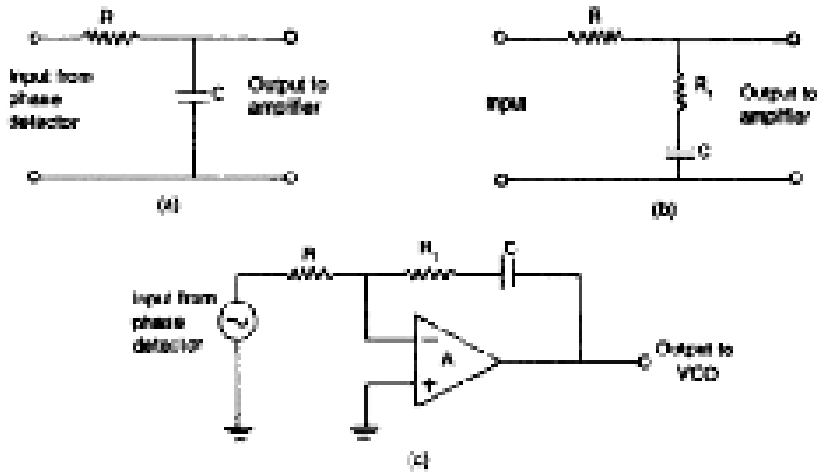


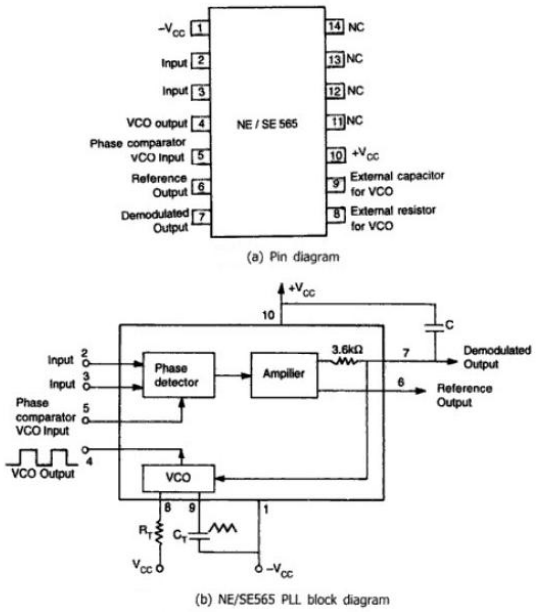
Figure 3.30

3.3.6 Monolithic PLL (IC565)

565 is available as a 14-pin DIP package and as 10-pin metal can package. The pin configuration and the block diagram are shown in Fig. 3.31(a, b). The output frequency of the VCO (both inputs 2, 3 grounded) can be rewritten as

$$f_o = \frac{0.25}{R_T C_T} Hz$$

where R_T and C_T are the external resistor and capacitor connected to pin 8 and pin 9. A value between 2 kΩ and 20 kΩ is recommended for R_T. The VCO free running frequency is adjusted with R_T and C_T to be at the centre of the input frequency range. It may be seen that phase locked loop is internally broken between the VCO output and the phase comparator input. A short circuit between pins 4 and 5 connects the VCO output to the phase comparator so as to compare f_s with input signal f_o. A capacitor C is connected between pin 7 and pin 10 (supply terminal) to make a low pass filter with the internal resistance of 3.6 kΩ.



(a) Pin diagram

(b) NE/SE565 PLL block diagram

Figure 3.31

The important electrical parameters of 565 PLL are:

Operating frequency range	:	0.001 Hz to 500 kHz
Operating voltage range	:	±6 V to ±12 V
Input level	:	10 mV rms min. to 3 V pp max
Input impedance	:	10 kΩ typical
Output sink current	:	1 mA typical
Drift in VCO centre frequency with temperature	:	300 ppm/°C. (parts per million per degree centigrade)
Drift in VCO centre frequency with supply voltage	:	1.5 per cent/V max
Triangle wave amplitude	:	2.4 V_{pp} at ±6 V supply voltage
Square wave amplitude	:	5.4 V_{pp} at ±6 V supply voltage
Bandwidth adjustment range	:	< ±1 to ±60%

3.3.7 Applications of PLL

The PLL can be used in a wide variety of applications, including (1) frequency demodulation, (2) frequency synthesis, and (3) FSK demodulation. Examples of each of these follow.

FM Demodulation:

If PLL is locked to a FM signal, the VCO tracks the instantaneous frequency of the input signal. The filtered error voltage which controls the VCO and maintains lock with the input signal is the demodulated FM output. The VCO transfer characteristics determine the linearity of the demodulated output. Since, VCO used in IC PLL is highly linear, it is possible to realize highly linear FM demodulators.

Frequency Synthesizer:

A frequency synthesizer can be built around a PLL as shown in Fig. 3.32. A frequency divider is inserted between the VCO output and the phase comparator so that the loop signal to the comparator is at frequency f_o while the VCO output is Nf_o. This output is a multiple of the input frequency as long as the loop is in lock. The input signal can be stabilized at f_1 with the resulting VCO output at Nf_1 if the loop is set up to lock at the fundamental frequency (when *fo* _ *f*1). Figure 17.27b shows an example using a 565 PLL as frequency multiplier and a 7490 as divider. The input *Vi* at frequency *f*1 is compared to the input (frequency *fo*) at pin 5. An output at *Nfo* (4*fo* in the present example) is connected through an inverter circuit to provide an input at pin 14 of the 7490, which varies between 0 and -5 V. Using the output at pin 9, which is divided by 4 from that at the input to the 7490, the signal at pin 4 of the PLL is four times the input frequency as long as the loop remains in lock. Since the VCO can vary over only a limited range from its center frequency, it may be necessary to change the VCO frequency whenever the divider value is changed. As long as the PLL circuit is in lock, the VCO output frequency will be exactly *N* times the input frequency. It is only necessary to readjust *fo* to be within the capture-and-lock range, the closed loop then resulting in the VCO output becoming exactly *Nf*1 at lock.

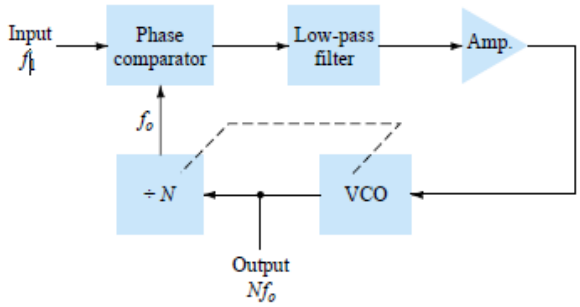


Figure 3.32

Frequency Shift Keying (FSK) Demodulator

In digital data communication and computer peripheral, binary data is transmitted by means of a carrier frequency which is shifted between two preset frequencies. This type of data transmission is called frequency shift keying (FSK) technique. The binary data can be retrieved using a FSK demodulator at the receiving end. The 565 PLL is very useful as a FSK demodulator. Figure 3.33 shows FSK demodulator using PLL for tele-typewriter signals of 1070 Hz and 1270 Hz. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding de shift at the output. A three stage filter removes the carrier component and the output signal is made logic compatible by a voltage comparator.

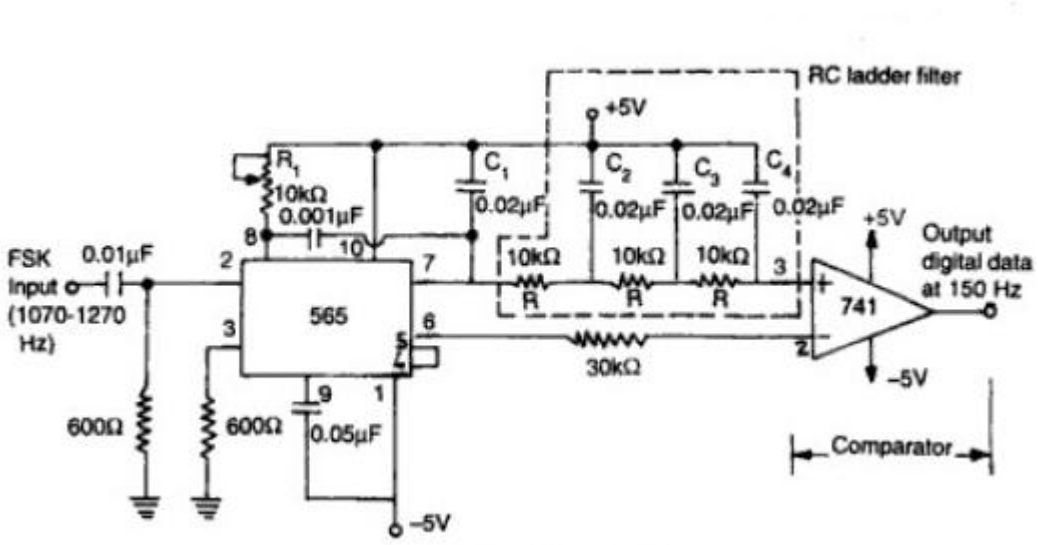


Figure 3.33

UNIT IV
VOLTAGE REGULATOR & D to A AND A to D CONVERTERS

VOLTAGE REGULATOR: Introduction, Series Op-Amp regulator, IC Voltage Regulators, IC 723 general purpose regulators, Switching Regulator. D to A AND A to D CONVERTERS: Introduction, basic DAC techniques -weighted resistor DAC, R-2R ladder DAC, inverted R-2R DAC, A to D converters -parallel comparator type ADC, counter type ADC, successive approximation ADC and dual slope ADC, DAC and ADC Specifications

4.1 Voltage Regulators

4.1.1 Introduction:

The function of a voltage regulator is to provide a stable de voltage for powering other electronic circuits. A voltage regulator should be capable of providing substantial output current. Voltage regulators are classified as:

- Series regulator
- Switching regulator

Series regulators use a power transistor connected in series between the unregulated de input and the load. The output voltage is controlled by the continuous voltage drop taking place across the series pass transistor. Since the transistor conducts in the active or linear region, these regulators are also called linear regulators. Linear regulators may have fixed or variable output voltage and could be positive or negative. The schematic, important characteristics, data sheet, short circuit protection, current fold-back, current boosting techniques for linear voltage regulators such as 78 XX, 79 XX series, 723 IC are discussed. Switching regulators, on the other hand, operate the power transistor as a high frequency on/off switch, so that the power transistor does not conduct current continuously. This gives improved efficiency over series regulator.

4.1.2 SERIES OP-AMP REGULATOR

A voltage regulator is an electronic circuit that provides a stable de voltage independent of the load current, temperature and ac line voltage variations. Figure 4.1 shows a regulated power supply using discrete components. The circuit consists of following four parts:

1. Reference voltage circuit

2. Error amplifier

3. Series pass transistor

4. Feedback network.

It can be seen from Fig. 4.1 that the power transistor Q_1 is in series with the unregulated dc voltage V_{in} and the regulated output voltage V_o. So it must absorb the difference between these two voltages whenever any fluctuation in output voltage V_{in} occurs. The transistor Q_1 is also connected as an emitter follower and therefore provides sufficient current gain to drive the load. The output voltage is sampled by the R-R divider and fed back to the (-) input terminal of the op-amp error amplifier. This sampled voltage is compared with the reference voltage V_{ref} (usually obtained by a zener diode). The output V_o of the error amplifier drives the series transistor Q_1.

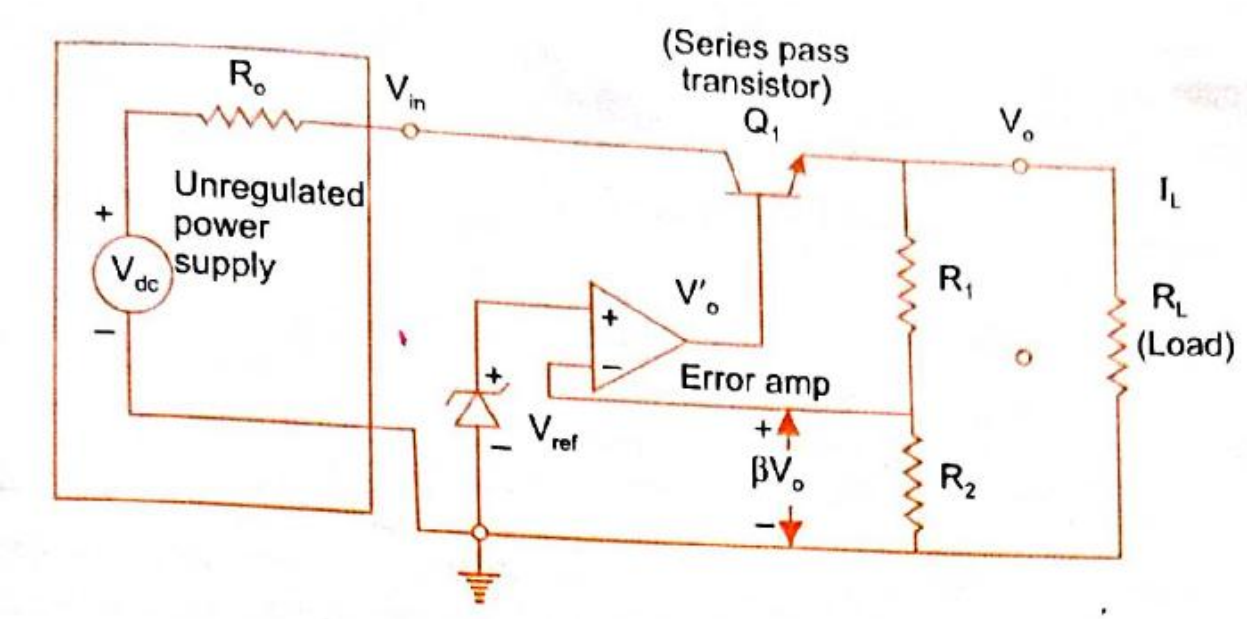


Figure 4.1

If the output voltage increases, say, due to variation in load current, the sampled voltage βV_o also increases where

$$\beta = \frac{R_2}{R_1 + R_2}$$

This, in turn, reduces the output voltage V of the diff-amp due to the 180° phase difference provided by the op-amp amplifier. V is applied to the base of Q1, which is used as an emitter follower. So Vo follows V, that is V, also reduces. Hence the increase in V, is nullified. Similarly, reduction in output voltage also gets regulated.

4.1.3 IC VOLTAGE REGULATORS

With the advent of micro-electronics, it is possible to incorporate the complete circuit of Fig. 4.1 on a monolithic silicon chip. This gives low cost, high reliability, reduction in size and excellent performance. Examples of monolithic regulators are 78 XX/79 XX series and 723 general purpose regulators.

Fixed Voltage Series Regulator

78 XX series are three terminal, positive fixed voltage regulators. There are seven output voltage options available such as 5, 6, 8, 12, 15, 18 and 24 V. In 78 XX, the last two numbers XX) indicate the output voltage. Thus 7815 represents a 15 V regulator. There are also available 79 XX series of fixed output, negative voltage regulators which are complements to the 78 XX series devices. There are two extra voltage options of - 2 V and – 5.2 V available in 79 XX series. These regulators are available in two types of packages.

Metal package (TO – 3 type)
Plastic package (TO - 220 type)

Figure 4.2 shows the standard representation of monolithic voltage regulator. A capacitor effects due to long distribution leads. The output capacitor C, (1 μF) improves the transient C; (0.33 μF) is usually connected between input terminal and ground to cancel the inductive response.

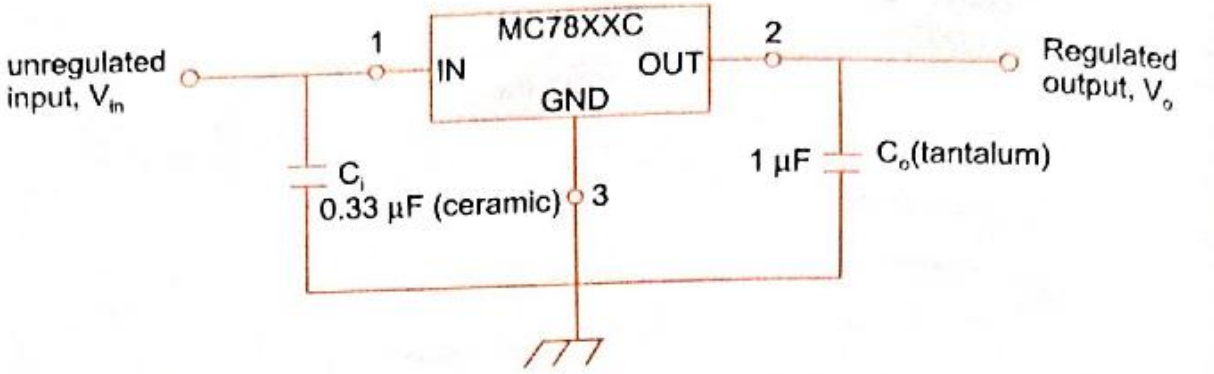


Figure 4.2

National Semiconductor also produces three terminal voltage regulators in the LM series. There are three series available for different operating temperature ranges:

- LM 100 series - 55°C to +125°C
- LM 200 series -25°C to 0°C
- LM 300 series +85°C to +70°C

The popular series are LM 340 positive regulators and LM 320 negative regulators with output ratings comparable to 78 XX/79 XX series.

Characteristics

There are four characteristics of three terminal IC regulators which must be mentioned.

1. V_o The regulated output voltage is fixed at a value as specified by the manufacturer. There are a number of models available for different output voltages, for example, 78 XX series has output voltage at 5, 6, 8 etc.

2. $V_{in} \geq V_o + 2$ volts: The unregulated input voltage must be atleast 2 V more than the regulated output voltage. For example, if $V_o = 5$ V, then $V_{in} = 7$ V.

3. $I_{o\,(max)}$: The load current may vary from 0 to rated maximum output current. The IC is usually provided with a heat sink, otherwise it may not provide the rated maximum output current.

4. Thermal shutdown: The IC has a temperature sensor (built-in) which turns off the IC when it becomes too hot (usually 125° C to 150°C). The output current will drop and remains there until the IC has cooled significantly.

Some of the important performance parameters are explained as follows:

Line/Input Regulation

It is defined as the percentage change in the output voltage for a change in the input voltage. It is usually expressed in millivolts or as a percentage of the output voltage. Typical value of line regulation of 7805 is 3 mV.

Load Regulation

It is defined as the change in output voltage for a change in load current and is also expressed in millivolts or as a percentage of V_o.Typical value of load regulation for 7805 is 15 mV for 5 mA < I < 1.5 A.

Ripple Rejection

The IC regulator not only keeps the output voltage constant but also reduces the amount of ripple voltage. It is usually expressed in dB. Typical value for 7805 is 78 dB.

The Schematic diagram of MC 78 XX is shown in Fig. 4.3. The circuit consists of a reference voltage Vref. This circuit basically consists of level shifter with zener diode input and the transistor Q used as emitter follower buffer. The circuit enclosed in the shaded region is a difference amplifier consisting of a current mirror (Q4, Q5), and an active load (Q6, Q7, Q8). The combination of R1R2 forms the feedback network for sampling the output voltage. The sampled voltage is fed to one of the inputs of the difference amplifier. The Darlington pair Q'Q" forms series pass element Q1 of the circuit shown in Fig. 4.1.

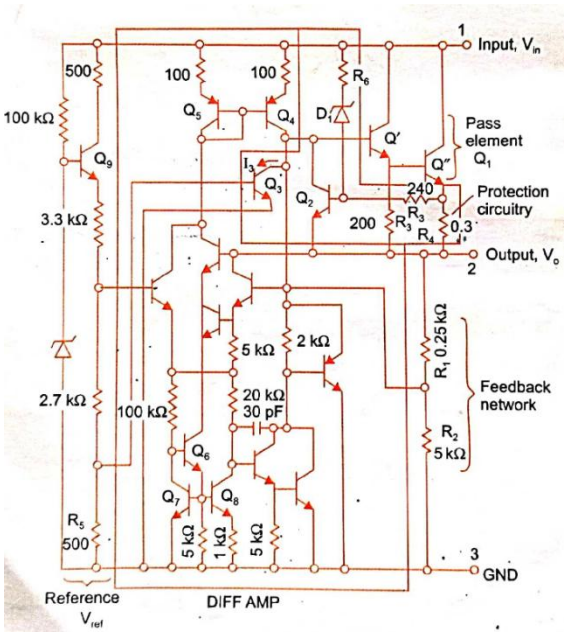


Figure 4.3

Current is limited by R3, R4 and transistor Q2. If the output voltage goes low due to overload, the excess voltage appears across the pass element (Q'-Q"), that is, across the collector emitter of Q". When this voltage is more than the break-down voltage of the zener drives it on. Now, because of the collector current of Q, when fully on, current flowing to diode D1, it starts conducting. This provides sufficient base current to transistor Q2 and the base of Q' is reduced. This in turn reduces the conduction of Q". Thus the volt-ampere product of the pass element (Q'-Q") is limited. The thermal overload protection is provided by the resistor R, and transistor Q3. The roltage drop across resistor R5 is directly applied to the base-emitter of Q3. When the temperature goes high, Q3 conducts more, thereby reducing the base drive of Q'Q" combination. This provides thermal protection.

Fixed Regulator used as Adjustable Regulator

In the laboratory, one may need variable regulated voltages or a voltage that is not available as a standard fixed voltage regulator. This can be achieved by using a fixed three terminals as shown in Fig.4.4 Note that the ground (GND) terminal of the fixed three terminal regulator is floating. The output voltage

$$V_o = \left(1 + \frac{R_2}{R_1}\right) V_R + R_2 I_Q$$

where V_R is the regulated voltage difference between the OUT and GND terminals. The effect of I_Q is minimized by choosing R_2 small enough to minimize the term $R_2 I_Q$. The minimum output voltage is the value of the fixed voltage available from the regulator. The LM117, 217, 317 positive regulators and LM137, 237, 337 negative regulators have been specially designed to be used for obtaining adjustable output voltages. It is possible to adjust output voltage from 1.2 V to 40 V and current upto 1.5 A.

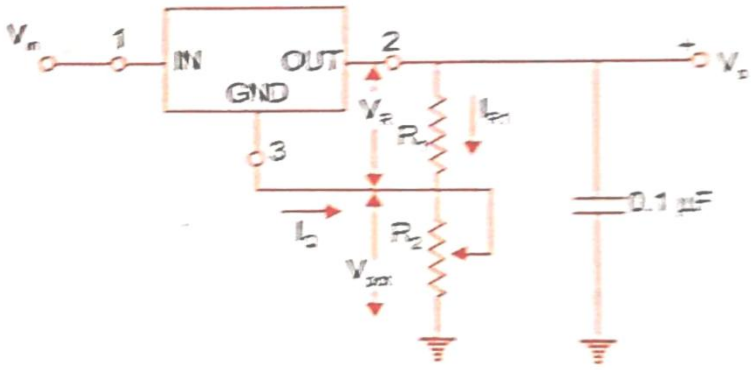


Figure 4.4

Dual Voltage Supply

Many discrete and IC circuits (such as op-amp) require bipolar (dual or ±V) supplies. This can be easily done with two three-terminal regulators. Figure 4.5 shows a bipolar ±15 V supply that can give 1 A from both (+) and (-) terminals. LM 340-15 is a +15V regulator with load current capability upto 1.5 A. The LM 320-15 is a -15 V regulator. It may be noted that the pin configuration of LM 340 and LM 320 is different. The diodes D1 and D2 in the circuit protect the regulator against short circuits occurring at its input terminals. Diodes D3 and D4 provide protection against the situation when both the regulators may not turn on simultaneously. If there is a load between the two outputs, the faster one will try to reverse the polarity of the other and cause it to latch up unless it is properly clamped. This clamping function is done by the diodes. Once the regulator starts operating properly, both diodes will be reverse biased and will no longer have any effect on the circuit.An op-amp draws less than 5 mA current, so a 100 mA supply can be used to drive a circuit consisting of 20 op-amps. LM 325H is a dual tracking ± 15V supply and is available in a 10-pin metal-can package and can furnish current upto 100 mA.

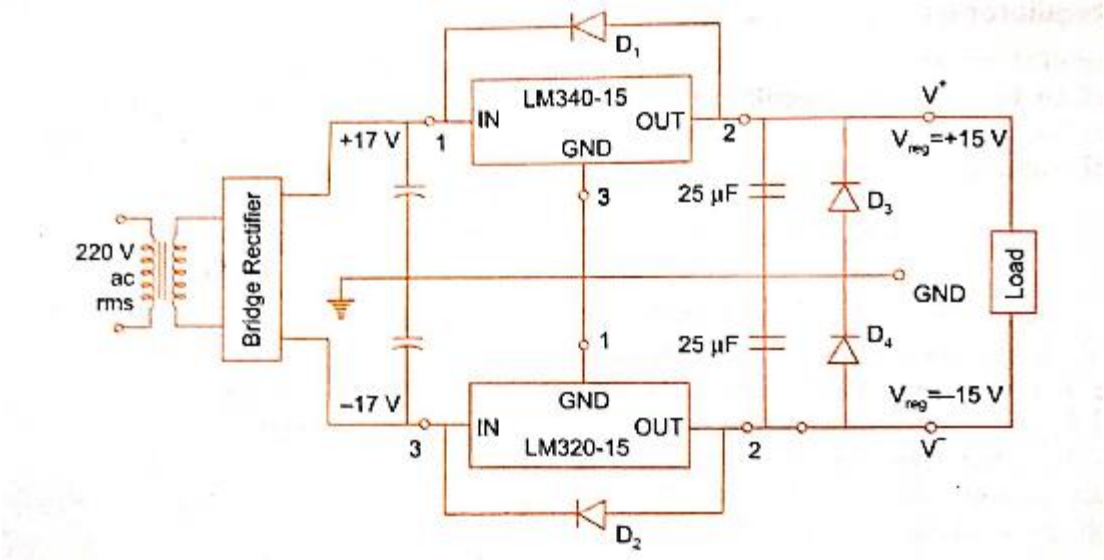


Figure 4.5

4.1.4 723 GENERAL PURPOSE REGULATOR

The three terminal regulators discussed earlier have the following limitations:

1. No short circuit protection
2. Output voltage (positive or negative) is fixed.

These limitations have been overcome in the 723 general purpose regulator, which can be adjusted over a wide range of both positive or negative regulated voltage. This IC is inherently low current device, but can be boosted to provide 5 amps or more current by connecting external components. The limitation of 723 is that it has no in-built thermal protection. It also has no short circuit current limits. Figure 4.6 (a) shows the functional block diagram of a 723 regulator IC. It has two separate sections. The zener diode, a constant current source and reference amplifier produce a fixed voltage of about 7 volts at the terminal V_{ref} . The constant current source forces the zener to operate at a fixed point so that the zener outputs a fixed voltage.

The other section of the IC consists of an error amplifier, a series pass transistor Q1 and a current limit transistor Q2 The error amplifier compares a sample of the output voltage applied at the INV input terminal to the reference voltage Vref applied at the NI input terminal. The error

signal controls the conduction of Q1 These two sections are not internally connected but the various points are brought out on the IC package. 723 regulated IC is available in a 14-pin dual-in-line package or 10-pin metal-can as shown in Fig. 4.6 (b).

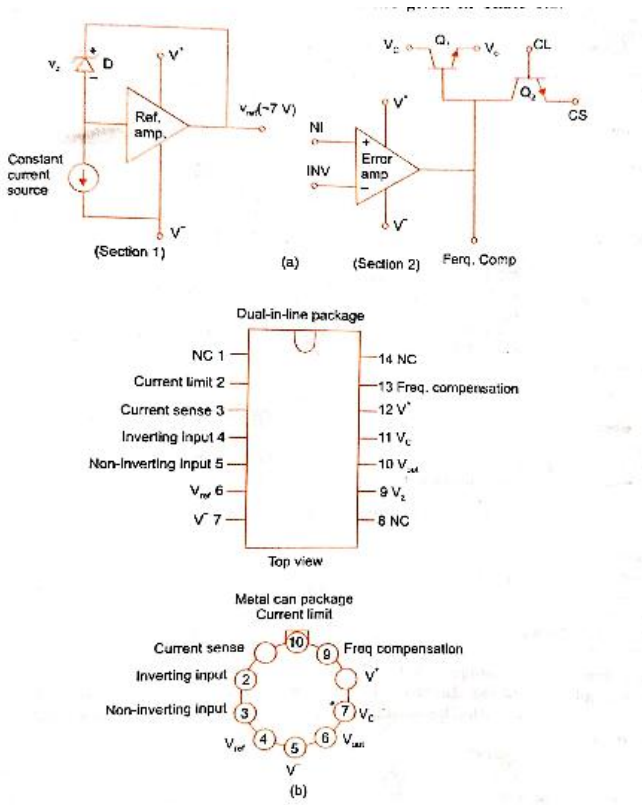


Figure 4.6

A simple positive low-voltage (2 V to 7V) regulator can be made using 723 as shown in the schematic of Fig. 4.7 (a). In order to understand the circuit operation, consider the detailed circuit of Fig.4.7 (b). The voltage at the NI terminal of the error amplifier due to R_1R_2 divider is

$$V_{NI} = V_{ref}\frac{R_2}{R_1 + R_2}$$

The difference between V_{NI} and the output voltage Vo which is directly fed back to the INV terminal is amplified by the error amplifier. The output of the error amplifier drives the pass transistor Q1 so as to minimize the difference between the NI and INV inputs of the error amplifier. Since Q1 is operating as an emitter follower

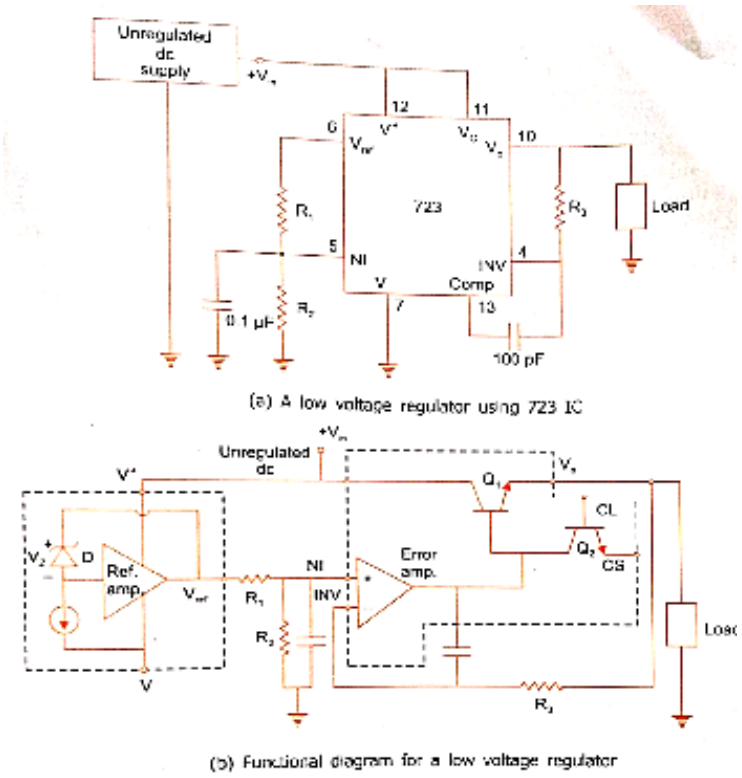
$$V_O = V_{ref} \frac{R_2}{R_1 + R_2}$$

If the output voltage becomes low, the voltage at the INV terminal of the error amplifier also goes down. This makes the output of the error amp to become more positive, thereby driving transistor Q, more into conduction. This reduces the voltage across Q1 and drives more current into the load causing voltage across load to increase. So the initial drop in the load stage has been compensated. Similarly, any increase in load voltage, or changes in the put voltage gets regulated.

The reference voltage is typically 7.15 V. So the output voltage V_O is

$$V_O = 7.15 \times \frac{R_2}{R_1 + R_2}$$

which will always be less than 7.15 V. So in the circuit of Fig. 6.8 (a) is used as low voltage (<7 V) 723 regulator.



(a) A low voltage regulator using 723 IC

(b) Functional diagram for a low voltage regulator

Figure 4.7

4.1.5 SWITCHING REGULATOR

The regulated power supplies discussed so far are referred to as linear voltage regulator, since the series pass transistor operates in the linear region. The linear voltage regulator has the following limitations.

The input step down transformer is bulky and the most expensive component of the linear regulated power supply mainly because of low line frequency (50 Hz). Because of the low line frequency, large values of filter capacitors are required to decrease the ripple. The efficiency of a series regulator is usually very low (typically 50 per cent). The input voltage must be greater than the output voltage. The greater the difference in input-output voltage, more will be the power dissipated in the series pass transistor which is always in the active region. A TTL system regulator (V = 5 V) when operated at 10 V dc input gives 50 per cent efficiency and only 25 per cent for 20 V dc input. Another limitation is that in a system with one dc supply voltage (such as

+5 V for TTL) if there is need for ±15 V for op-amp operation, it may not be economically and practically feasible to achieve this.

Switched mode power supplies overcome these difficulties. The switching regulator, also called switched mode regulator operate in a significantly different way from that of a conventional series regulator circuit discussed earlier. In series regulator, the pass transistor is operated in its linear region to provide a controlled voltage drop across it with a steady de current flow. Whereas, in the case of switched-mode regulator, the pass transistor is used as a "controlled switch" and is operated at either cutoff or saturated state. Hence the power transmitted across the pass device is in discrete pulses rather than as a steady current flow. Greater efficiency is achieved since the pass device is operated as a low impedance switch. When the pass device is at cutoff, there is no current and dissipates no power. Again when the pass device is in saturation, a negligible voltage drop appears across it and thus dissipates only a small amount of average power, providing maximum current to the load. In either case, the power wasted in the pass device is very little and almost all the power is transmitted to the load. Thus efficiency in switched mode power supply is remarkably high-in the range of 70-90%.

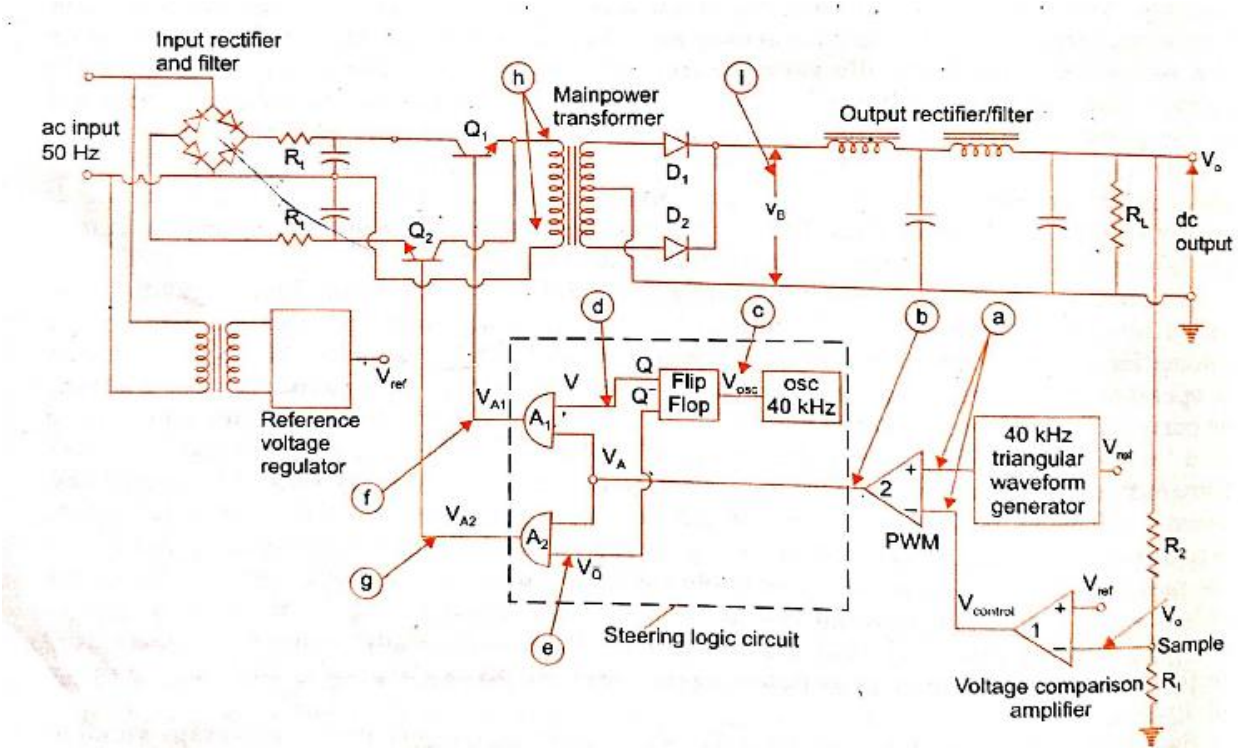


Figure 4.8

Switched mode regulators rely on pulse width modulation to control the average value of output voltage. The average value of a repetitive pulse waveform depends on the area under the waveform.. A switching power supply is shown in Fig.. The bridge rectifier and capacitor filters are connected directly to the ac line to give unregulated de input. The thermistor R limits the high initial capacitor charge current. The reference regulator is a series pass regulator of the type shown in Fig. 4.8. Its output is a regulated reference voltage Vref which serves as a power supply voltage for all other circuits. The current drawn from Vref is usually very small (~10 mA), so the power loss in the series pass regulator switched not affect the overall efficiency of the switched mode power supply (SMPS). Transistors Q1 and Q2 are alternately switched off and on at 20 kHz. These transistors are either fully on (V_{CE} sat 0.2 V) or cut-off, so they dissipate very little power. These transistors drive the primary of the main transformer. The secondary is centre-tapped and full wave rectification is achieved by diodes D1 and D2. This unidirectional square wave is next filtered through a two stage LC filter to produce output voltage Vo. The regulation of Vin is achieved by the feedback circuit consisting of a pulse-width modulator and steering logic circuit. The output voltage Vo is sampled by a R1R2 divider and a fraction (R2/R1+R2) is compared with a fixed reference voltage Vref in comparator 1. The output of this stage comparison amplifier is called $V_{control}$ and is shown in Fig. 4.9 (a). $V_{control}$ is applied to the (-) input terminal of comparator 2 and a triangular waveform of frequency 40 kHz is shown in Fig. 4.9 (a) is applied at the (+) input terminal. It may be noted that a high frequency triangular waveform is being used to reduce the ripple. The comparator 2 functions as a pulse width modulator and its output is a square wave V_A (Fig. 6.14 (b)) of period T_f 40 kHz). The duty cycle of the square wave is T1/(T1+ T2) and varies with Vcontrol which turn varies with the variation of $v_{\circ}$. The output VA drives a steering logic circuit shown the dashed block. It consists of a 40 kHz oscillator cascaded with a flip-flop to produce shown in Fig. 4.9 (d) and (e). The output V_{A1} and complementary outputs V_{A2} of AND gates A1 and A2 are shown in Fig.4.9 (f) and (g). These waveforms are applied the base of transistor Q1 and Q2. Depending upon whether transistor Q1 or Q is on, the waveform at the input of the transformer will be a square wave as shown in Fig. 6.14 (h). è rectified output up is shown in Fig. 6.14 (i).

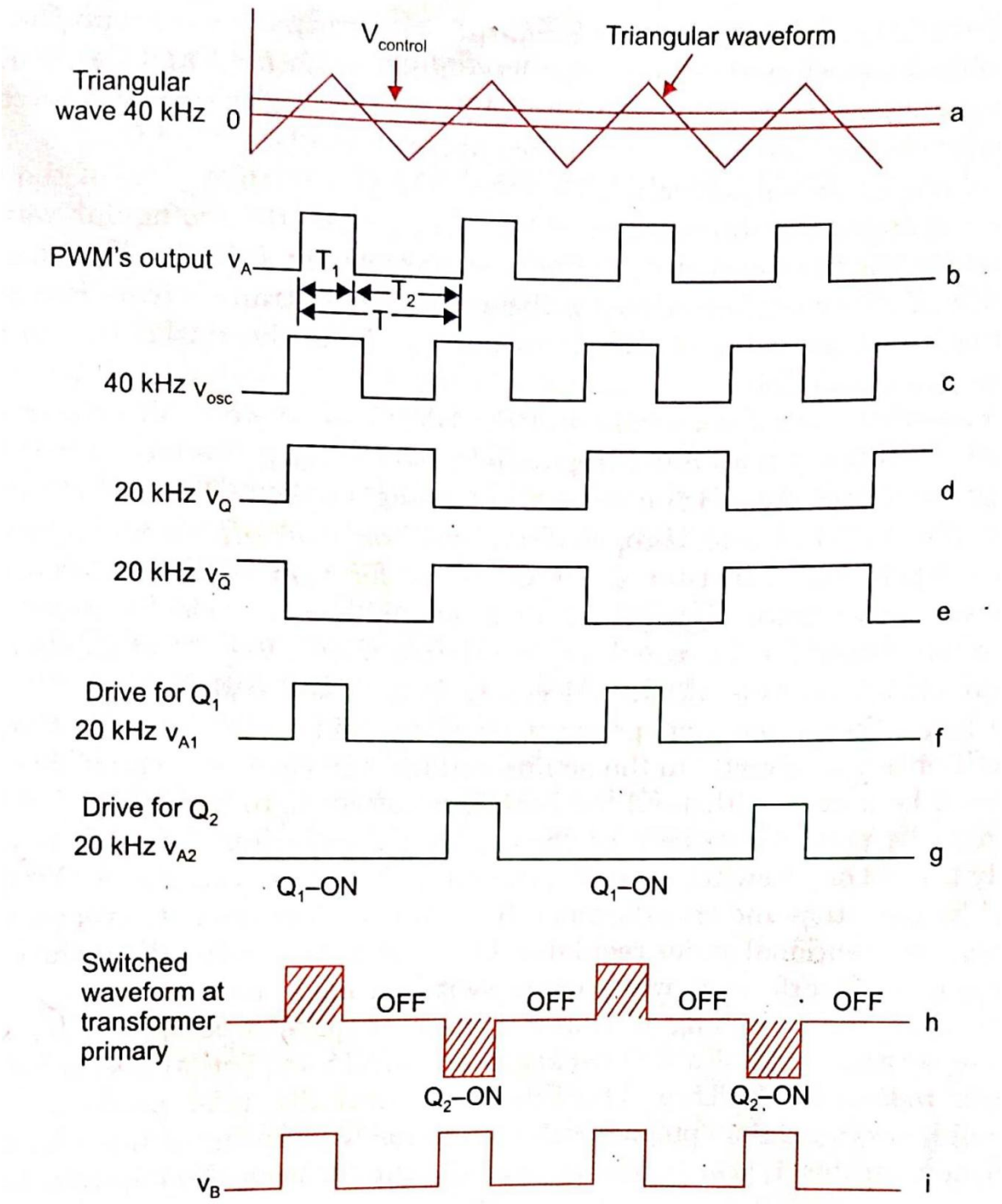


Figure 4.9

An inspection of Fig. 4.8 shows that the output current passes through the power switch a switch with low losses (transistor with small $V_{CE\ (sat)}$ and high switching speed) and a filter consisting of transistors Q, and Q, an inductor having low resistance and the load. Hence using

With a high quality factor, the conversion efficiency can easily exceed 90%. If there is a rise in dc output voltage V, the voltage control $V_{control}$ of the comparator 1
also rises. This changes the intersection of the $V_{control}$ with the triangular waveform and in the pulse width of the waveform driving the main power transformer. Reduction in pulse in this case decreases the time period T, in the waveform of Fig. 4.9(b). This in turn decreases width and lowers the average value of the dc output V.. Thus the initial rise in the dc output
voltage V has been nullified.

So far we have discussed the operation of the SMPS. Now we shall be able to justify why SMPS has better efficiency than linear regulated power supply. We have noted that very high frequency signals (about 40 kHz or more) are being applied. The transistors Q1 and Q are acting as the switches and become alternately on and off at a frequency of 20 kHz (Fig.4.9 (a)). Again the transistor Q1 or Q, is on for very small duration and consumes negligibly small power since $V_{CE\ (sat)}$ (0.2V) is small. It may also be noted that the high operating frequency used for the switching transistors allows the use of smaller transformers, capacitors and inductors. This allows a decrease in size and cost.

There are some limitations and precautions to be taken with switching power supplies. Since the rectifier is tied directly to the ac line voltage, the rectifiers, capacitors and switching transistors must be able to withstand the peak line voltage (310 V for 220 V ac rms line). The resistor R, must be provided to prevent the uncharged capacitors from shorting out the line when initially turned on. A switched mode power supply is more complex and requires external components like inductors and transformers. It is slow in responding to transient load changes compared to the conventional series regulator. One should be careful about the electromagnetic and radio-frequency interference while using switched mode power supply.

As can be seen, the switching regulator system is quite a complex one. However, with modern microelectronics, quite a few packages are available. The Motorola MC 3420/3520 is a pulse width modulator IC chip. The Silicon General SG 1524 produces an IC package containing

reference regulator, pulse width modulator (consisting of saw tooth oscillator and comparator), comparator 1, transistors Q1 and Q2, the steering flip-flop and two AND gates.

4.2 D to A and A to D converters

4.2.1 Introduction:

Most of the real-world physical quantities such as voltage, current, temperature, pressure and time etc. are available in analog form. Even though an analog signal represents a real physical parameter with accuracy, it is difficult to process, store or transmit the analog signal without introducing considerable error because of the superim-position of noise as in the case of amplitude modulation. Therefore, for processing, transmission and storage purposes, it is often convenient to express these variables in digital form. It gives better accuracy and reduces noise. The operation of any digital communication system is based upon analog to digital (A/D) and digital to analog (D/A) conversion.

Figure 4.10 highlights a typical application within which A/D and D/A conversion is used. The analog signal obtained from the transducer is band limited by antialiasing filter. The signal is then sampled at a frequency rate more than twice the maximum frequency of the band limited signal. The sampled signal has to be held constant while conversion is taking place in A/D converter. This requires that ADC should be preceded by a sample and hold (S/H) circuit. The ADC output is a sequence in binary digit. The micro-computer or digital signal processor performs the numerical calculations of the desired control algorithm. The D/A converter is to convert digital signal into analog and hence the function of DAC is exactly opposite to that of ADC. The D/A converter is usually operated at the same frequency as the ADC. The output of a D/A converter is commonly a staircase. This staircase-like digital output is passed through a smoothing filter to reduce the effect of quantization noise.

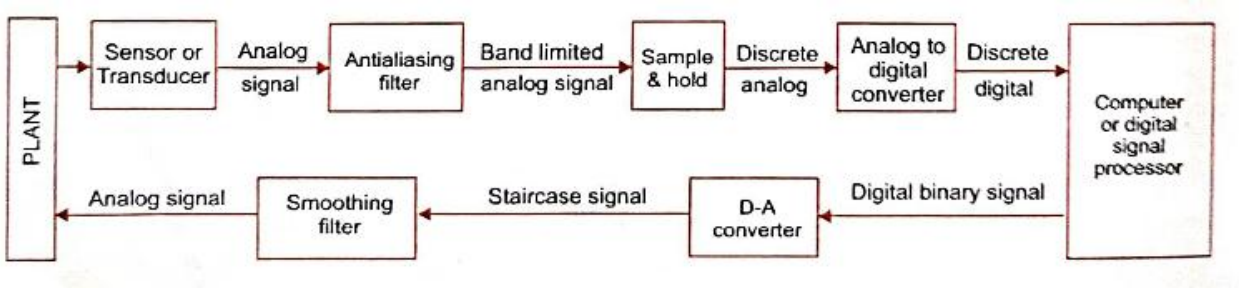


Figure 4.10

The scheme given in Fig. 4.10 is used either in full or in part in applications such as digital audio recording and playback, computer, music and video synthesis, pulse code modulation transmission, data acquisition, digital multimeter, direct digital control, digital signal processing, microprocessor based instrumentation.

Both ADC and DAC are also known as data converters and are available in IC form. It may be mentioned here that for slowly varying signal, sometimes sample and hold circuit may be avoided without considerable error. The A-D conversion usually makes use of a D-A converter so we shall first discuss DAC followed by ADC

4.2.2 Basic DAC techniques

The schematic of a DAC is shown in Fig. 4.11 The input is a 2-bit binary word D and is combined with a reference voltage V_R to give an analog output signal. The output of a DAC can be either a voltage or current. For a voltage output DAC, the D/A converter is mathematically described as

$V_0 = V_{FS} K(d_1 2^{-1} + d_2 2^{-2} + \ldots\ldots\ldots\ldots\ldots + d_n 2^{-n})$

K = scaling factor usually adjusted to unity

V_0 = output voltage

V_{FS} = full scale output voltage

d_n= most significant bit (MSB)

d_1 = least significant bit (LSB)

There are various ways to implement Eq. (10.1). Here we shall discuss the following resistive techniques only:

- Weighted resistor DAC
- R-2R ladder
- Inverted R-2R ladder

4.2.3 Weighted Resistor DAC

One of the simplest circuits shown in Fig. 4.12 (a) uses a summing amplifier with a binary weighted resistor network. It has n-electronic switches d1, d2,., dn controlled by binary input word. These switches are single pole double throw (SPDT) type. If the binary input to a particular switch is 1, it connects the resistance to the reference voltage (V_R). And if the input bit is 0, the switch connects the resistor to the ground. From Fig. 4.12(a), the output voltage for an ideal op-amp can be written as,

$$V_0 = V_R \frac{R_f}{R}(d_1 2^{-1} + d_2 2^{-2} + \ldots\ldots\ldots\ldots\ldots + d_n 2^{-n})$$

The circuit shown in Fig.4.12 (a) uses a negative reference voltage. The analog output voltage is therefore positive staircase as shown in Fig. 4.12 (b) for a 3-bit weighted resistor DAC. It may be noted that

(i) Although the op-amp in Fig. 4.12(a) is connected in inverting mode, it can also be connected in non-inverting mode.

(ii) The op-amp is simply working as a current to voltage converter.

(iii) The polarity of the reference voltage is chosen in accordance with the type of the switch used. For example, for TTL compatible switches, the reference voltage should be +5 V and the output will be negative.

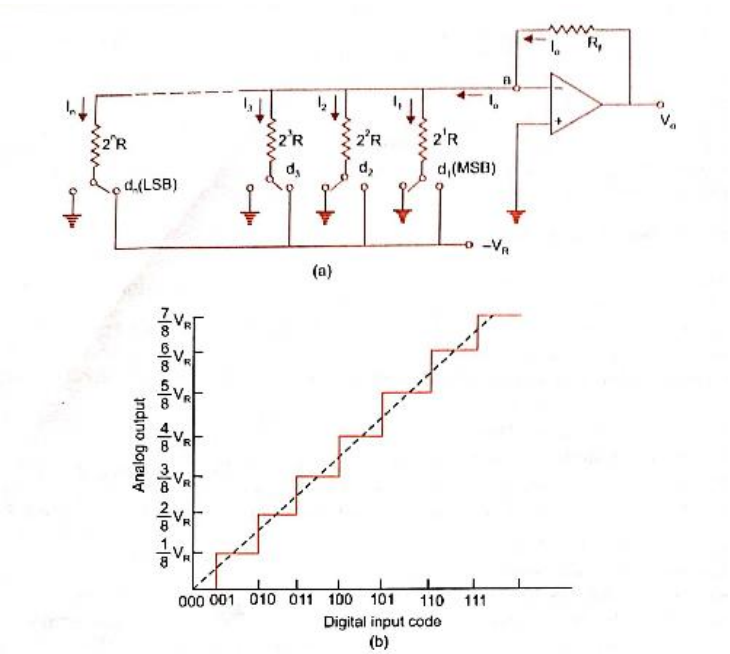


Figure 4.12

4.2.4 R-2R Ladder DAC

Wide range of resistors are required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC where only two values of resistors are required. It is well suited for integrated circuit realization. The typical value of R ranges from 2.5 k to 10 kn.

For simplicity, consider a 3-bit DAC as shown in Fig.4.13 (a), where the switch position di dads corresponds to the binary word 100. The circuit can be simplified to the equivalent form of Fig. 4.13 (b) and finally to Fig. 4.13 (c).

The output voltage is

$$V_o = \frac{-2R(-V_R)}{R(4)}$$

$$V_o = \frac{V_R}{2}$$

$$V_o = \frac{V_{FS}}{2}$$

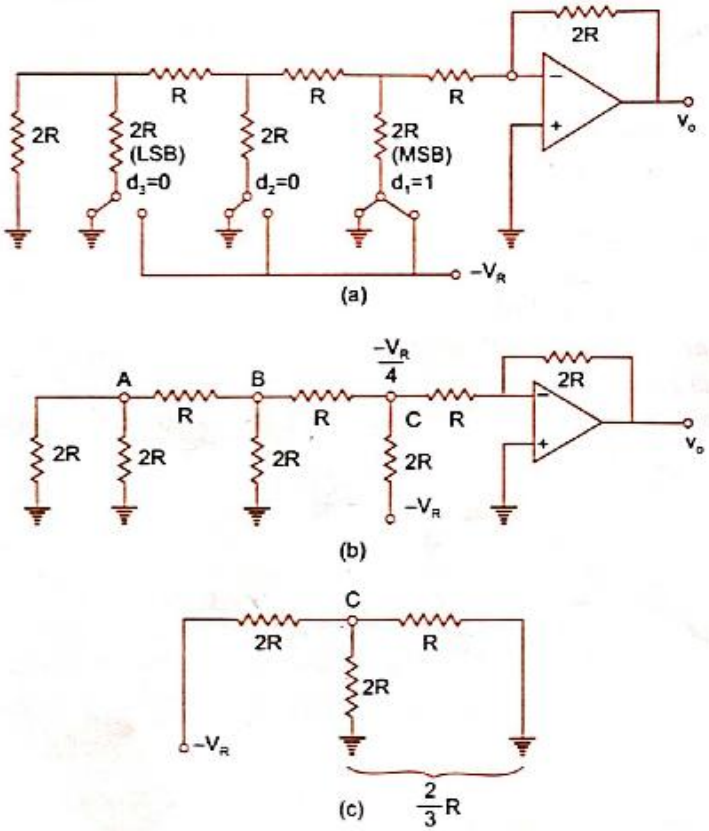


Figure 4.13

4.2.5 Inverted R-2R Ladder

In weighted resistor type DAC and R-2R ladder type DAC, current flowing in the resistors changes as the input data changes. More power dissipation causes heating, which in turn, creates non-linearity in DAC. This is a serious problem and can be avoided completely in Inverted R-2R ladder type DAC. A 3-bit Inverted R-2R ladder type DAC is shown in Fig. 4.13 (a) where the position of MSB and LSB is interchanged. Here each input binary word connects the corresponding switch either to ground or to the inverting input terminal of the op-amp which is also at virtual ground. Since both the terminals of switches d; are at ground potential, current flowing in the resistances is constant and independent of switch position, i.e. independent of input binary word. In Fig.4.13(a), when switch d; is at logical i.e., to the left, the current through

2R resistor flows to the ground and when the switch d; is at logical '1' i.e., to the right, the current through 2R sinks to the virtual ground. The circuit has the important property that the current divides equally at each of the nodes. This is because the equivalent resistance to the right or to the left of any node is exactly 2 R. The division of the current is shown in Fig.4.13 (b). Consider a reference current of 2 mA. Just to the right of node A, the equivalent resistor is 2 R. Thus 2 mA of reference input current divides equally to value 1 mA at node A. Similarly to the right of node B, the equivalent resistor is 2 R. Thus 1 mA of current further divides to value 0.5 mA at node B. Similarl current divides equally at node C to 0.25 mA. The equal division of current in successive nodes remains the same in the inverted R-2R ladder; irrespective of the input binary word. Thus the currents remain constant in each branch of the ladder. Since constant current implies constant voltage, the ladder node voltages remain constant at $V_R/2°$, $V_R/2^1$, $V_R/2^2$. The circuit works on the principle of summing currents and is also said to operate in the current mode. The most important advantage of the current mode or inverted ladder is that since the ladder node voltages remain constant even with changing input binary words (codes), the stray capacitances are not able to produce slow-down effects on the performance of the circuit. It may be noted that the switches used in Fig.4.13 (a) are the SPDT switches discussed earlier. According to bit d, the corresponding switch gets connected either to ground for d = 0 or to $-V_R$ for $d_i = 1$. The current flows from inverting input terminal to $-V_R$ for d; = 1 and from ground to $-V_R$ for d; = 0. Regardless of the binary input word, the current in the resistive branches of the inverted ladder circuit remains always constant as explained in Fig.4.13(b). However, the current through the feedback resistor R is the summing current depending upon the input binary word. It may further be mentioned that, Fig.4.13 (b) shows only the current division for making the analysis simple, though it is a voltage driven DAC.

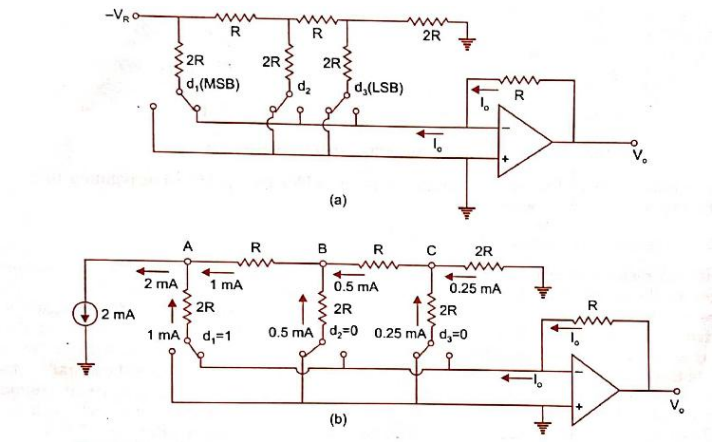


Figure 4.13

4.2.6 A to D converters

The block schematic of ADC shown in Fig.4.14 provides the function just opposite to that of DAC. It accepts an analog input voltage Vin and produces an output binary word d_n of functional value D .An ADC usually has two additional control lines: the START input to tell the ADC when to start the conversion and the EOC (end of conversion) output to announce when the conversion is complete. Depending upon the type of application, ADCs are designed for microprocessor interfacing or to directly drive LCD or LED displays.

ADCs are classified broadly into two groups according to their conversion technique. Direct type ADCs and Integrating type ADCs. Direct type ADCs compare a given analog signal with the internally generated equivalent signal. This group includes

- Flash (comparator) type converter
- Counter type converter
- Tracking or servo converter
- Successive approximation type converter

Integrating type ADCs perform conversion in an indirect manner by first changing the analog input signal to a linear function of time or frequency and then to a digital code. The two most widely used integrating type converters are:

- Charge balancing ADC
- Dual slope ADC

The most commonly used ADCs are successive approximation and the integrator type. The successive approximation ADCs are used in applications such as data loggers and

instrumentation where conversion speed is important. The successive approximation and comparator type are faster but generally less accurate than integrating type converters. The flash (comparator) type is expensive for high degree of accuracy. The integrating type converter is used in applications such as digital meter, panel meter and monitoring systems where the conversion accuracy is critical.

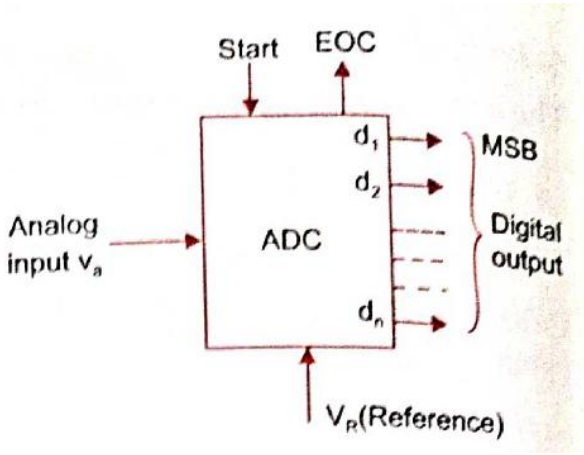
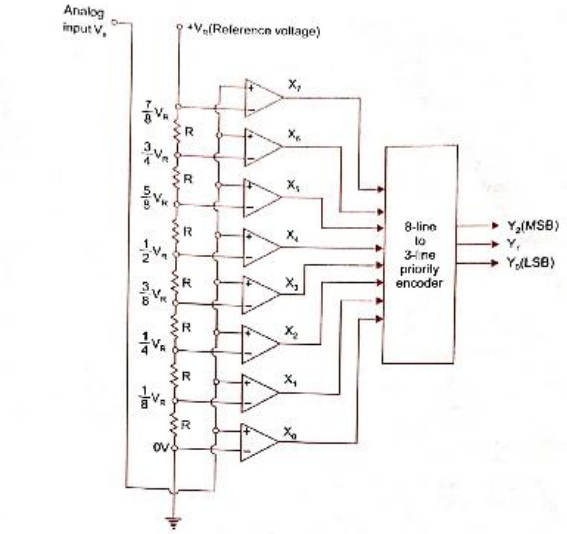


Figure 4.14

4.2.7 The Parallel Comparator (Flash) A/D Converter

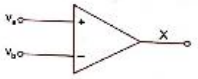
This is the simplest possible A/D converter. It is at the same time, the fastest and most expensive technique. Figure4.15 (a) shows a 3-bit A/D converter. The circuit consists of a resistive divider network, 8 op-amp comparators and a 8-line to 3-line encoder (3-bit priority encoder). The comparator and its truth table is shown in Fig.4.15 (b). A small amount of hysteresis is built into the comparator to resolve any problems that might occur if both inputs were of equal voltage as shown in the truth table. Coming back to Fig. 4.15(a), at each node of the resistive divider, a comparison voltage is available. Since all the resistors are of equal value, the voltage levels available at the nodes are equally divided between the reference voltage VR and the ground. The purpose of the circuit is to compare the analog input voltage V with each of the node voltages. The truth table for the flash type AD converter is shown in Fig.4.15(c). The circuit has the advantage of high speed as the conversion take place simultaneously rather than sequentially. Typical conversion time is 100 ns or less. Conversion time is limited only by the speed of the comparator and of the priority encoder. By using an Advanced Micro Devices AMD

686A comparator and a T1147 priority encoder, conversion delays of the order of 20 ns can be obtained. This type of ADC has the disadvantage that the number of comparators required almost doubles for each added bit. A 2-bit ADC requires 3 comparators, 3-bit ADC needs 7, whereas 4-bit requires 15 comparators. In general, the number of comparators required are where n is the desired number of bits. Hence the number of comparators approximately doubles for each added bit. Also the larger the value of n, the more complex is the priority encoder.



(a) Basic circuit of a flash type A/D converter

Voltage input	Logic output X
$V_a > V_d$	$X = 1$
$V_a < V_d$	$X = 0$
$V_a = V_d$	Previous value



(b) Comparator and its truth table

Input voltage V_a	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ to $V_R/4$	0	0	0	0	0	0	1	1	0	0	1
$V_R/4$ to 3 $V_R/8$	0	0	0	0	0	1	1	1	0	1	0
3 $V_R/8$ to $V_R/2$	0	0	0	0	1	1	1	1	0	1	1
$V_R/2$ to 5 $V_R/8$	0	0	0	1	1	1	1	1	1	0	0
5 $V_R/8$ to 3 $V_R/4$	0	0	1	1	1	1	1	1	1	0	1
3 $V_R/4$ to 7 $V_R/8$	0	1	1	1	1	1	1	1	1	1	0
7 $V_R/8$ to V_R	1	1	1	1	1	1	1	1	1	1	1

(c) Truth table for a flash type A/D converter

Figure 4.15

4.2.8 The Counter Type A/D Converter

The D /A converter can easily be turned around to provide the inverse function A to D conversion. The principle is to adjust the DAC input code until the DAC output comes within+(1/2) LSB to the analog input V which is to be converted to binary digital form. Thus in

addition to the DAC, we need suitable logic circuitry to perform the code search and a comparator of adequate quality to announce when the DAC output has come within +(1/2) LSB to V.A 3-bit counting ADC based upon the above principle is shown in Fig.4.16 (a). The counter is reset to zero count by the reset pulse. Upon the release of RESET, the clock pulses are counted by the binary counter. These pulses go through the AND gate which is enabled by the voltage comparator high output. The number of pulses counted increase with time. The binary word representing this count is used as the input of a D/A converter whose output is a staircase of the type shown in Fig.4.16 (b). The analog output Va of DAC is compared to the analog input Va by the comparator. If V_a greater than Vd, the output of the comparator becomes high and the AND gate is enabled to allow the transmission of the clock pulses to the counter. When Va less than V_d, the output of the comparator becomes low and the AND gate is disabled. This stops the counting at the time Va ≤ Va and the digital output of the counter represents the analog input voltage Va. For a new value of analog input V1, a second reset pulse is applied to clear the counter. Upon the end of the reset, the counting begins again.

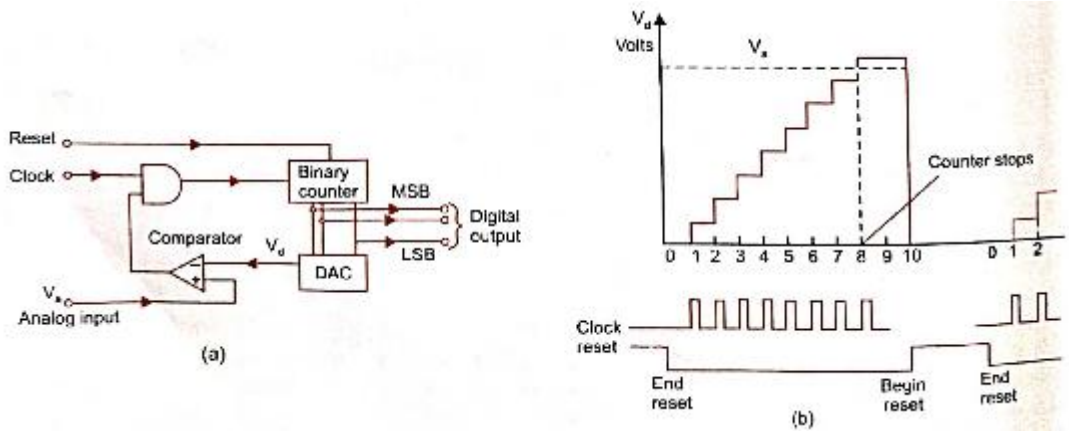


Figure 4.16

4.2.9 Successive Approximation Converter

The successive approximation technique uses a very efficient code search strategy to complete -bit conversion in just n-clock periods. An eight bit converter would require eight clock pulses to obtain a digital output. Figure 4.17 shows an eight bit converter. The circuit uses a successive approximation register (SAR) to find the required value of each bit by trial and error. The circuit operates as follows. With the arrival of the START command, = 1 with all other the SAR sets the MSB d1 bits to zero so that the trial code is 10000000. The output V_a of the DAC is

now compared with analog input V. If Va is greater than the DAC output Va then 10000000 is less than the correct digital representation. The MSB is left and the next lower significant bit is made 1 and further tested. However, if Va is less than the DAC output, then 10000000 is greater than the correct digital representation. So reset MSB to 0 and go on to the next lower significant bit. This procedure is repeated for all subsequent bits, one at a time, until all bit positions have been tested. Whenever the DAC output crosses V,, the comparator changes state and thi can be taken as the end of conversion (EOC) command. Figure 4.18 shows a typical conversion sequence

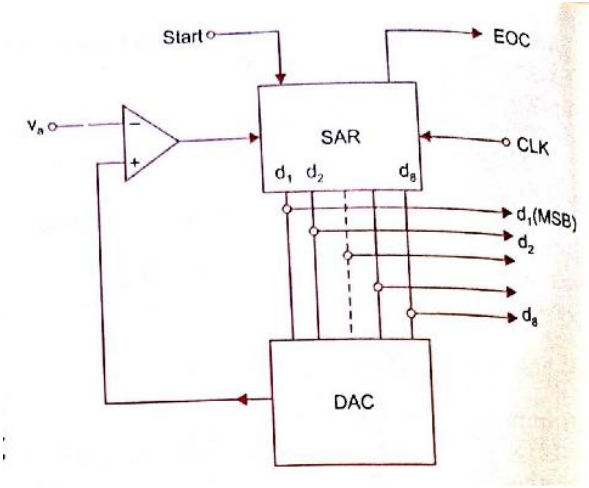


Figure 4.17

Correct digital representation	Successive approximation register output V_d at different stages in conversion	Comparator output
11010100	10000000	1 (initial output)
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	

Figure 4.18

4.2.10 Dual-Slope ADC

Figure 4.19 (a) shows the functional diagram of the dual-slope or dual-ramp converter. The analog part of the circuit consists of a high input impedance buffer A1, precision integrator

4, and a voltage comparator. The converter first integrates the analog input signal V1 for a fixed duration of clock periods as shown in Fig. 4.19 (b). Then it integrates an internal reference voltage VR of opposite polarity until the integrator output is zero. The number N of clock cycles required to return the integrator to zero is proportional to the value of Va averaged over the integration period. Hence N represents the desired output code. The circuit operates as follows:

Before the START command arrives, the switch SW, is connected to ground and SW2 is closed. Any offset voltage present in the A1, A2, comparator loop after integration, appears across the capacitor C till the threshold of the comparator is achieved. The capacitor C thus provides automatic compensation for the input-offset voltages of all the three amplifiers. Later, when SW2 opens, C acts as a memory to hold the voltage required to keep the offset nulled. At the arrival of the START command at t = t1, the control logic opens SW2 and connects SW1 to V, and enables the counter starting from zero. The circuit uses an n-stage ripple counter and therefore the counter resets to zero after counting pulses. The analog voltage Va is integrated for a fixed number counts of clock pulses after which the counter resets to zero. If the clock period is T, the integration takes place for a time T1 = 2T and the output is a ramp going downwards as shown in Fig. 4.19(b). The counter resets itself to zero at the end of the interval T1 and the switch SW1 is connected to the reference voltage (V_R). The output voltage $v_\circ$ will now have a positive slope. As long as v, is negative, the output of the comparator is positive and the control logic allows the clock pulse to be counted. However, when u, becomes just zero at time t = t3, the control logic issues an end of conversion (EOC) command and no further clock pulses enter the counter. It can be shown that the reading of the counter at t is proportional to the analog input voltage Va.

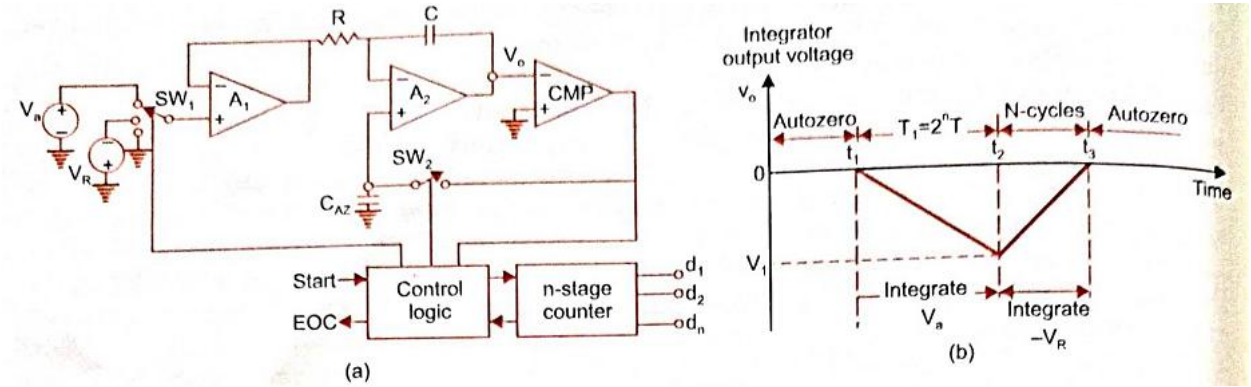


Figure 4.19

Dual-slope converters are particularly suitable for accurate measurement of slowly varying signals, such as thermocouples and weighing scales. Dual-slope ADCs also form the basis of digital panel meters and multimeters.

Dual-slope converters are available in monolithic form and are available both in microprocessor compatible and in display oriented versions. The former provide the digital code in binary form whereas the display oriented versions present the output code in a format suitable for the direct drive of LED displays. The Datel Intersil ICL7109 is a monolithic 12-bit dual-slope ADC with microprocessor compatibility.

4.2.11 DAC/ADC SPECIFICATIONS

Both D/A and A/D converters are available with wide range of specifications. The various important specifications of converters generally specified by the manufacturers are analyzed.

Resolution:

The resolution of a converter is the smallest change in voltage which produced at the output (or input) of the converter. For example, an 8-bit D/A converter has 2^8-1 = 255 equal intervals. Hence the smallest change in output voltage is (1/255) of the full scale output range. In short, the resolution is the value of the LSB. However, resolution is stated in a number of different ways. An 8-bit DAC is said to have

- : 8 bit resolution
- : a resolution of 0.392 of full-scale
- : a resolution of 1 part in 255

Similarly, the resolution of an A/D converter is defined as the smallest change in analog input for a one bit change at the output. As an example, the input range of an 8-bit A/D converter is divided into 255 intervals. So the resolution for a 10 V input range is 39.22 mV (= 10 V/255). Table below gives the resolution for 6-16 bit DACs.

Bits	Intervals	LSB size (% of Full Scale)	LSB size (10 V Full Scale)
6	63	1.588	158.8 mV
8	256	0.392	39.2 mV
10	1023	0.0978	9.78 mV
12	4095	0.0244	2.44 mV
14	16383	0.0061	0.61 mV
16	65535	0.0015	0.15 mV

Linearity:

The linearity of an A/D or D/A converter is an important measure of its accuracy and tells us how close the converter output is to its ideal transfer characteristics. In an ideal DAC, equal increment in the digital input should produce equal increment in the analog output and the transfer curve should be linear. However, in an actual DAC, output voltages do not fall on a straight line because of gain and offset errors as shown by the solid line curve in Fig. 4.20

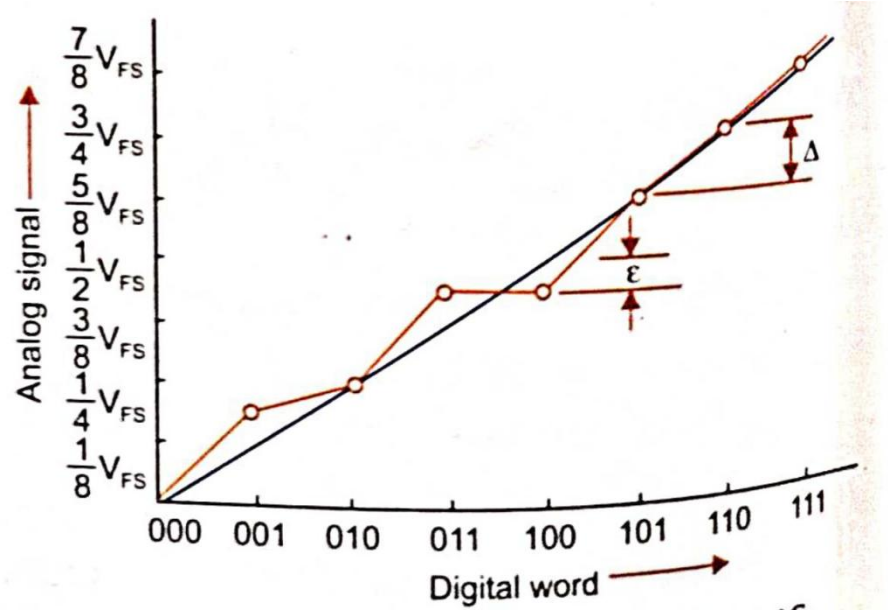


Figure 4.20

fitting a straight line through the measured output points. The linearity error measures the deviation of the actual output from the fitted line and is given by E/A as shown in Fig.4.20. The error is voltage. A good converter exhibits a linearity error of less than ± (1/2) LSB.

Accuracy: Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output. Relative accuracy is the maximum deviation after gain and offset errors have been removed. Data sheets normally specify relative accuracy rather than absolute accuracy. The accuracy of a converter is also specified in terms of LSB
increments or percentage of full scale voltage

Monotonicity: A monotonic DAC is the one whose analog output increases for an increase in digital input. Figure4.21 represents the transfer curve for a non-monotonic DAC, since the output decreases when input code changes from 001 to 010. A monotonic characteristic is essential in control applications, otherwise oscillations can result. In successive approximation ADCs, a non-monotonic characteristic may lead to missing codes. If a DAC has to be monotonic, the error should be less than +(1/2) LSB at each output level. All the commercially available DACS are monotonic because the linearity error never exceeds +(1/2) LSB at each output level.

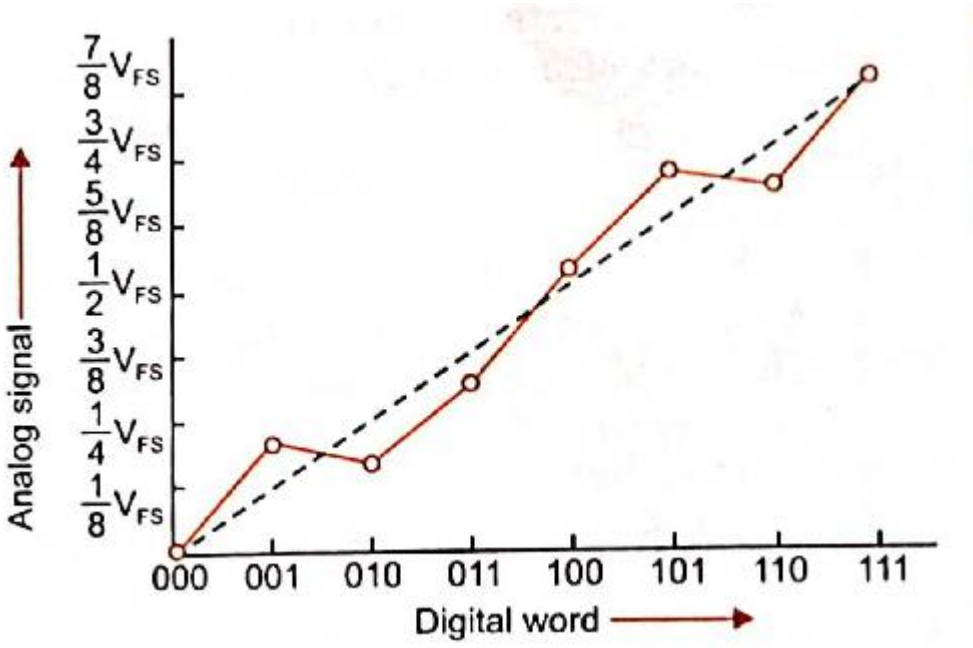


Figure 4.21

Settling time: The most important dynamic parameter is the settling time. It represents the time it takes for the output to settle within a specified band ±(1/2) LSB of its final value following a code change at, the input (usually a full scale change). It depends upon the switching time of the

logic circuitry due to internal parasitic capacitances and inductances. Settling time ranges from 100 ns to 10 us depending on word length and type of circuit used.

Stability: The performance of converter changes with temperature, age and power supply variations. So all the relevant parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges.

UNIT V

CMOS LOGIC, COMBINATIONAL CCIRCUITS USING TTL 74XX ICs & SEQUENTIAL CIRCUITS UNIT TTL 74XXICs

CMOSLOGIC : CMOS logic levels, MOS transistors, Basic CMOS Inverter, NAND and NOR gates, CMOSAND – OR – INVERT and OR - AND-INVERT gates, implementation of any function using CMOS logic.

COMBINATIONALCIRCUITSUSINGTTL74XXICs : Study of logic Gates using 74XXICs, Four-bit parallel adder(IC7483), Comparator(IC 7485), Decoder (IC 74138, IC 74154), BCD to 7-segment decoder(IC7447), Encoder(IC74147), Multiplexer(IC74151), Demultiplexer (IC74154).

SEQUENTIALCIRCUITSUSINGTTL74XXICs : Flip Flops(IC7474, IC7473), Shift Registers, Universal Shift Register(IC74194), 4-bit Asynchronous binary counter(IC7493).

5.1 CMOS Logic Family:

The CMOS (Complementary Metal Oxide Semiconductor) logic family uses both N-type and P-type MOSFETs (enhancement MOSFETs, to be more precise) to realize different logic functions. The main advantage of the CMOS logic family over bipolar logic families discussed so far lies in its extremely low power dissipation.

The CMOS logic family, like TTL, has a large number of subfamilies.

The basic difference between different CMOS logic subfamilies such as 4000A, 4000B, 4000UB, 74C, 74HC, 74HCT, 74AC and 74ACT is in the fabrication process used and not in the design of the circuits employed to implement the intended logic function.

5.2 Circuit Implementation of Logic Functions:

CMOS logic include inverter, NAND, NOR, AND, OR, EX-OR, EX-NOR and AND-OR-INVERT functions.

5.2.1 CMOS Inverter:

The inverter is the most fundamental building block of CMOS logic. It consists of a pair of N-channel and P-channel MOSFETs connected in cascade configuration as shown in Figure. The circuit.

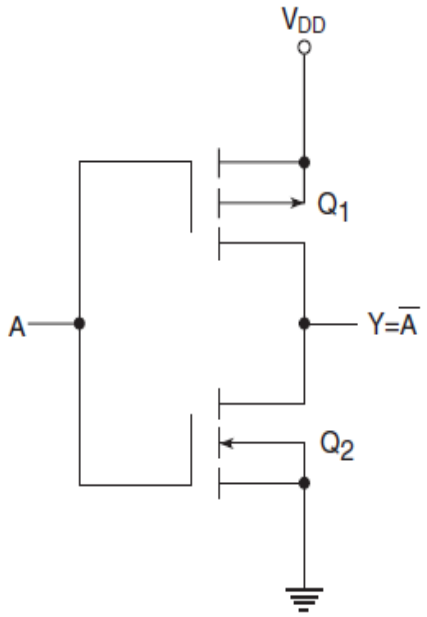


Figure 1

When the input is in the HIGH state (logic '1'), P-channel MOSFET Q_1 is in the cut-off state while the N-channel MOSFET Q_2 is conducting. The conducting MOSFET provides a path from ground to output and the output is LOW (logic '0').

When the input is in the LOW state (logic '0'), Q_1 is in conduction while Q_2 is in cut-off. The conducting P-channel device provides a path for V_{DD} to appear at the output, so that the output is in HIGH or logic '1' state.

A floating input could lead to conduction of both MOSFETs and a short-circuit condition. It should therefore be avoided. It is also evident from Figure that there is no conduction path between V_{DD} and ground in either of the input conditions, that is, when input is in logic '1' and '0' states.

That is why there is practically zero power dissipation in static conditions. There is only dynamic power dissipation, which occurs during switching operations as the MOSFET gate capacitance is charged and discharged. The power dissipated is directly proportional to the switching frequency.

5.2.2 NAND Gate:

As shown in the figure, two P-channel MOSFETs (Q_1 and Q_2 are connected in parallel between V_{DD} and the output terminal, and two N-channel MOSFETs (Q_3 and Q_4 are connected in series between ground and output terminal.

The circuit operates as follows. For the output to be in a logic '0' state, it is essential that both the series-connected N-channel devices conduct and both the parallel-connected P-channel devices remain in the cut-off state. This is possible only when both the inputs are in a logic '1' state.

This verifies one of the entries of the NAND gate truth table. When both the inputs are in a logic '0' state, both the N-channel devices are non conducting and both the P-channel devices are conducting, which produces a logic '1' at the output.

This verifies another entry of the NAND truth table. For the remaining two input combinations, either of the two N-channel devices will be nonconducting and either of the two parallel-connected P-channel devices will be conducting. We have either Q_3 OFF and Q_2 ON or Q_4 OFF and Q_1 ON.

The output in both cases is a logic '1', which verifies the remaining entries of the truth table.

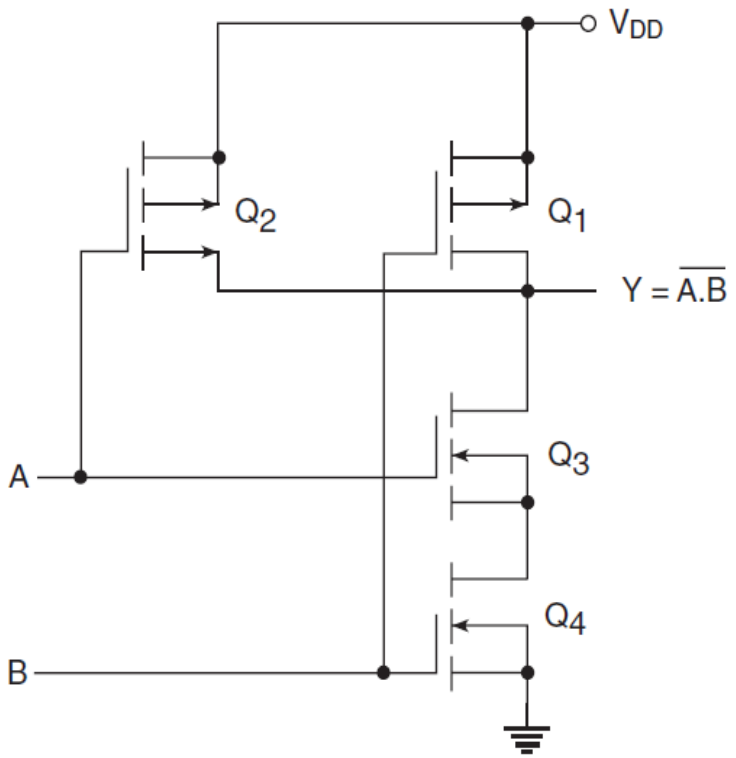


Figure 2 CMOS NAND

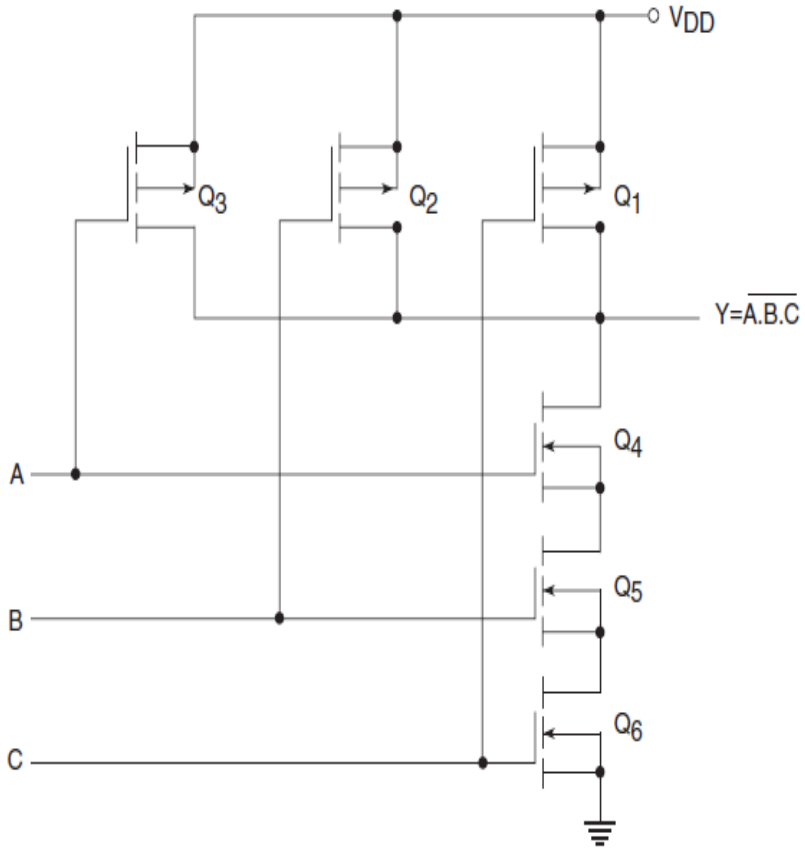


Figure 3 three - input NAND in CMOS

From the circuit schematic of Figure(2) we can visualize that under no possible input combination of logic states is there a direct conduction path between VDD and ground. This further confirms that there is near-zero power dissipation in CMOS gates under static conditions.

Figure(3) shows how the circuit of Figure(2) can be extended to build a three-input NAND gate. Operation of this circuit can be explained on similar lines.

It may be mentioned here that series connection of MOSFETs adds to the propagation delay, which is greater in the case of P-channel devices than it is in the case of N-channel devices. As a result, the concept of extending the number of inputs as shown in Figure(b) is usually limited to four inputs in the case of NAND and to three inputs in the case of NOR.

The number is one less in the case of NOR because it uses series-connected P-channel devices. NAND and NOR gates with larger inputs are realized as a combination of simpler gates

5.2.3 NOR Gate:

Figure(4) shows the basic circuit implementation of a two-input NOR. As shown in the figure, two P-channel MOSFETs (Q_1 and Q_2 are connected in series between V_{DD} and the output terminal, and two N-channel MOSFETs (Q_3 and Q_4 are connected in parallel between ground and output terminal. The circuit operates as follows.

For the output to be in a logic '1' state, it is essential that both the series-connected P-channel devices conduct and both the parallel-connected N-channel devices remain in the cut-off state. This is possible only when both the inputs are in a logic '0' state.

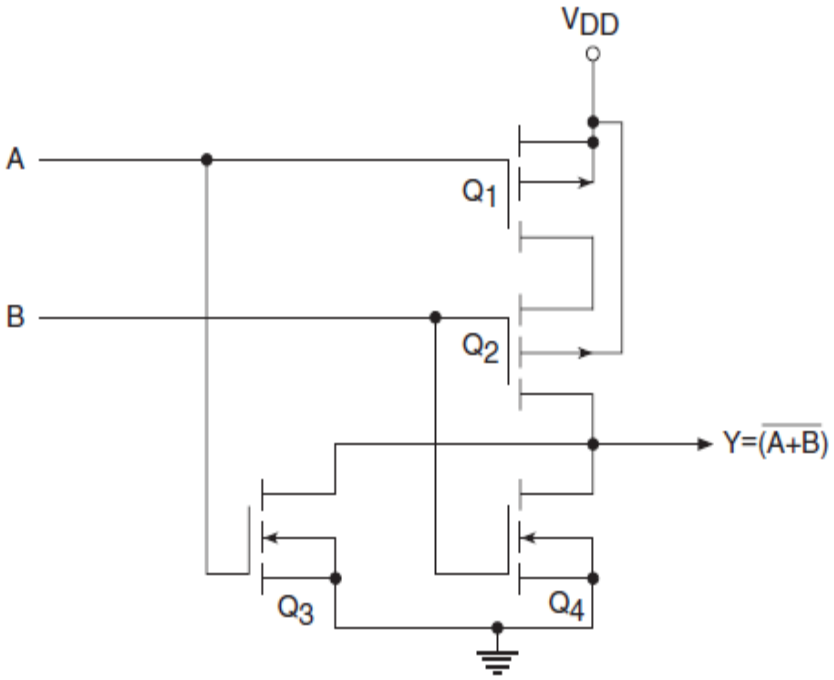


Figure 4 Two - input NOR in CMOS

This verifies one of the entries of the NOR gate truth table. When both the inputs are in a logic '1' state, both the N-channel devices are conducting and both the P-channel devices are nonconducting, which produces a logic '0' at the output.

This verifies another entry of the NOR truth table. For the remaining two input combinations, either of the two parallel N-channel devices will be conducting and either of the two series-connected P-channel devices will be nonconducting.

We have either Q_1 OFF and Q_3 ON or Q_2 OFF and Q_4 ON. The output in both cases is logic '0', which verifies the remaining entries of the truth table.

5.2.4 AND-OR-INVERT and OR-AND-INVERT Gates:

Figure 5.43 shows the internal schematic of a typical two-wide, two-input AND-OR-INVERT gate. The output of this gate can be logically expressed by the Boolean equation

$$Y = \overline{(A.B + C.D)}$$

From the above expression, we can say that the output should be in a logic '0' state for the following input conditions:

1. When either A.B=logic '1' or C.D=logic '1'
2. When both A.B and C.D equal logic '1'.

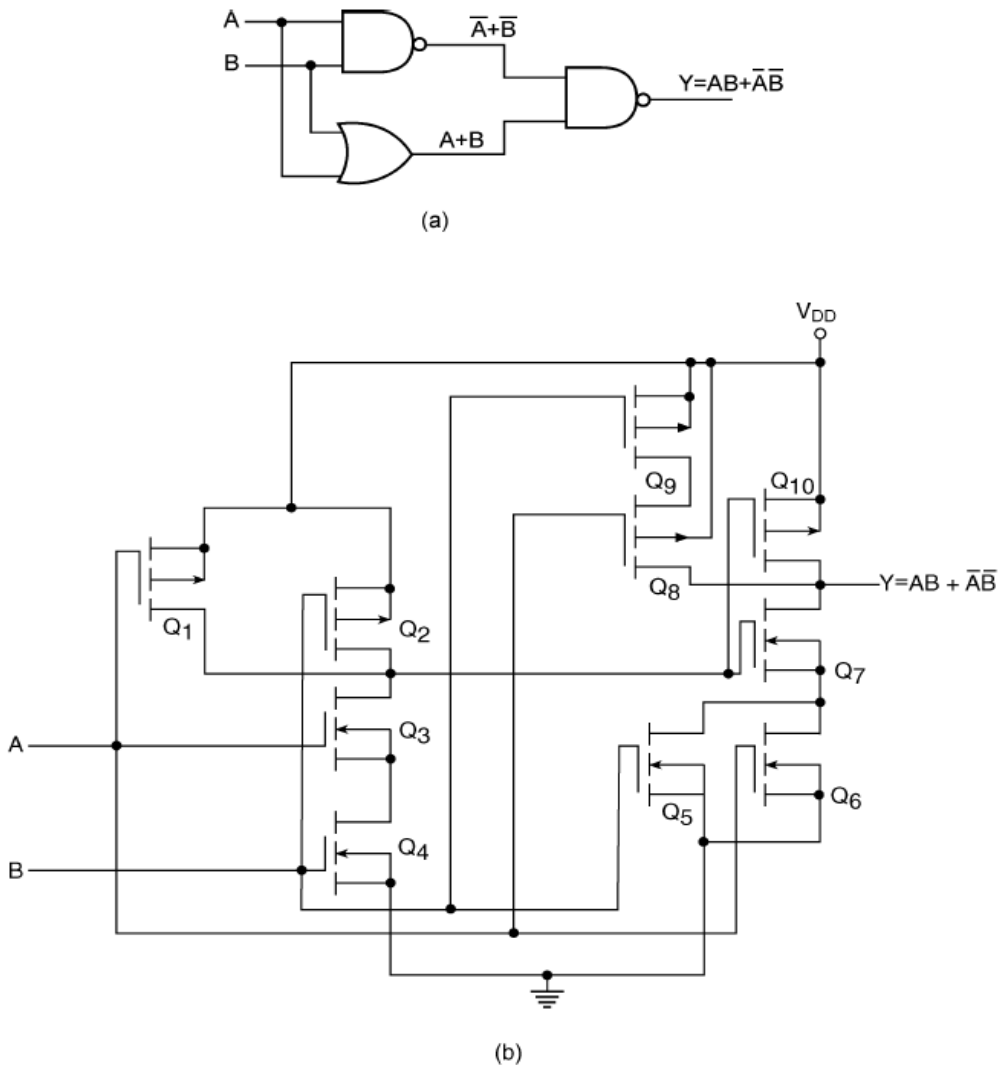


Figure 5 Two - input EX - NOR in CMOS

For both these conditions there is a conduction path available from ground to output, which verifies that the circuit satisfies the logic expression. Also, according to the logic expression for the AND-ORINVERT gate, the output should be in a logic '1' state when both A.B and C.D equal logic '0'. This implies that:

1. Either A or B or both are in a logic '0' state.
2. Either C or D or both are in a logic '0' state.

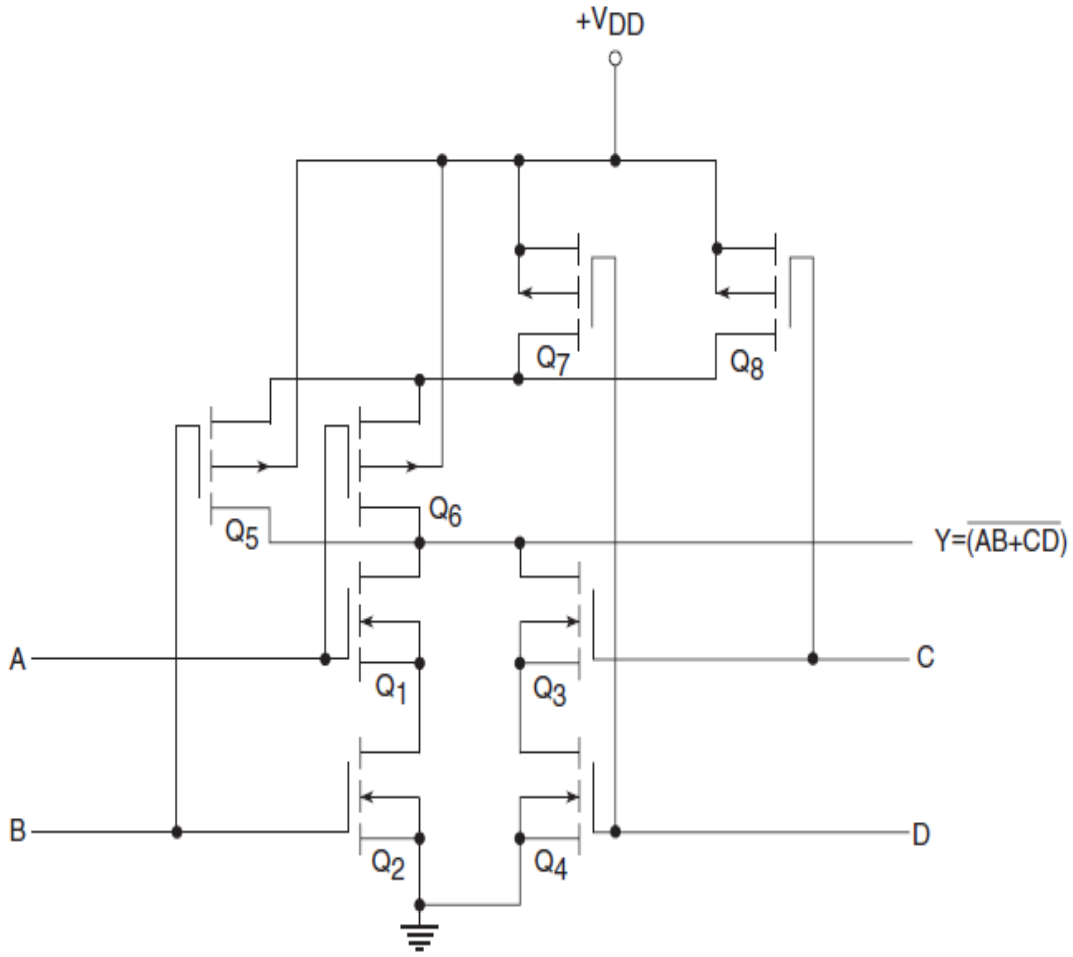


Figure 6 Two - wide AND - OR - INVERT gate in CMOS

If these conditions are applied to the circuit of Figure(6), we find that the ground will remain disconnected from the output and also that there is always a path from V_{DD} to output. This leads to a logic '1' at the output.

Thus, we have proved that the given circuit implements the intended logic expression for the AND-OR-INVERT gate.

The **OR-AND-INVERT** gate can also be implemented in the same way. Figure(7) shows a typical internal schematic of a two wide, two-input OR-AND-INVERT gate. The output of this gate can be expressed by the Boolean equation

$$Y = \overline{((A+B).(C+D))}$$

The circuit has two parts, that is, the N-channel MOSFET part of the circuit and the P-channel part of the circuit.

The two parallel arrangements are then connected in series to achieve an ANDing operation. The complementary P-channel MOSFET section achieves inversion. Note that the P-channel section is the complement of the N-channel section with N-channel MOSFETs replaced by P-channel MOSFETs and parallel connection replaced by series connection, and vice versa. The operation of an AND-OR-INVERT gate can be explained on similar lines to the case of an OR-AND INVERT gate.

Expansion of both AND-OR-INVERT and OR-AND-INVERT gates should be obvious, ensuring that we do not have more than three devices in series.

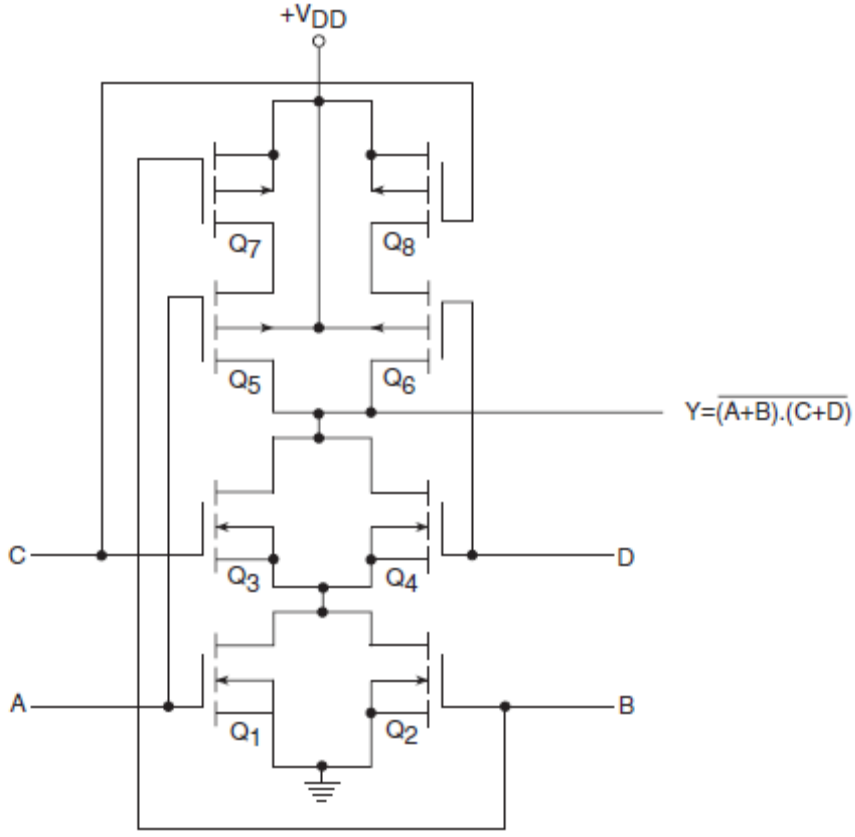


Figure 7 Two - wide, two - input OR - AND - INVERT gate

5.3 COMBINATIONALCIRCUITSUSINGTTL74XXICs:

5.3.1 Four-bit parallel adder (full adder) (IC7483):

A full adder circuit is an arithmetic circuit block that can be used to add three bits to produce a SUM and a CARRY output. Such a building block becomes a necessity when it comes to adding binary numbers with a large number of bits.

The full adder circuit overcomes the limitation of the half-adder, which can be used to add two bits only. Let us recall the procedure for adding larger binary numbers. We begin with the addition of LSBs of the two numbers.

We record the sum under the LSB column and take the carry, if any, forward to the next higher column bits. As a result, when we add the next adjacent higher column bits, we would be required to add three bits if there were a carry from the previous addition. We have a similar situation for the other higher column bits also until we reach the MSB. A full adder is therefore essential for the hardware implementation of an adder circuit capable of adding larger binary numbers. A half-adder can be used for addition of LSBs only.

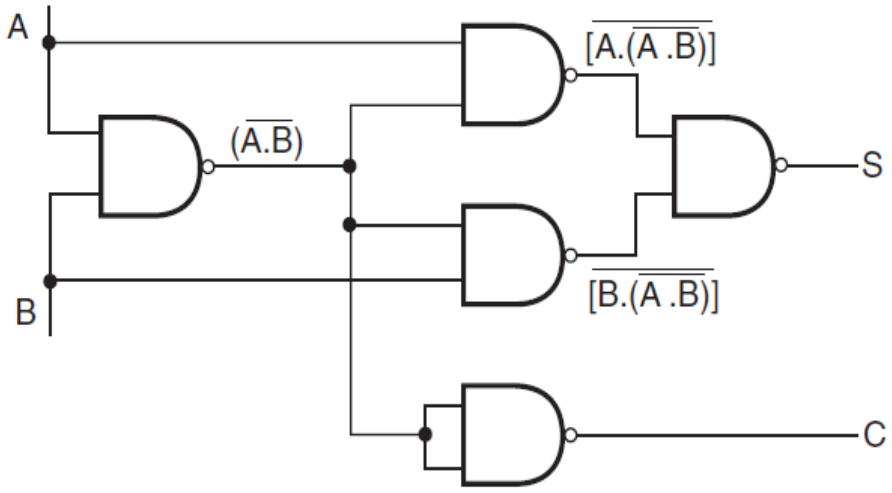
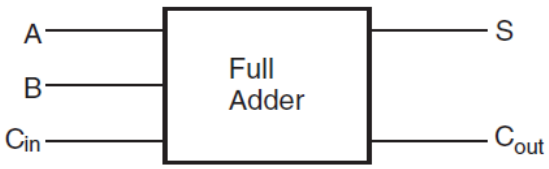


Figure 8 half - adder implementation using NAND gates.



A	B	C_{in}	SUM (S)	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 9 Truth table of the full adder

In order to arrive at the logic circuit for hardware implementation of a full adder, we will firstly write the Boolean expressions for the two output variables, that is, the SUM and CARRY outputs, in terms of input variables.

The Boolean expressions for the two output variables are given in Equation (1) for the SUM output (S) and in Equation (2) for the CARRY output (C_{out}):

$$S = \bar{A} \,.\, \bar{B} \,.C_{in} + \bar{A} \,.\, B.\, \bar{c}_{in} + A.\, \bar{B}\, \bar{c}_{in} + A \,.\, B \,.\, C_{in} \quad \text{(1)}$$

$$C_{out} = \bar{A} \,.\, B.\, C_{in} + A \,.\, \bar{B}\, C_{in} + A \,.\, B\, \bar{c}in + A \,.\, B \,.\, C_{in} \quad \text{(2)}$$

Using Karnaugh map for the above two expression,

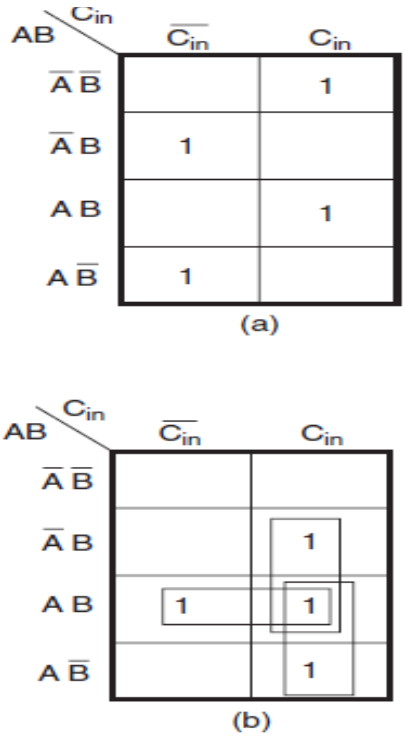


Figure 10 karnaugh maps for the sum and carry - out of a full adder

the simplified Boolean expression for Cout is given by the equation

$$C_{out} = B.C_{in} + A.B + A.C_{in} \quad \text{(3)}$$

The above equation represent the logic circuit diagram of the full adder.

A full adder can also be seen to comprise two half-adders and an OR gate. The expressions for SUM and CARRY outputs can be rewritten as follows

$$S = \bar{c}_{in}(\bar{A}.B + A.\bar{B}) + C_{in}.(A.B + \bar{A}.\bar{B})$$

$$S = \bar{c}_{in}(\bar{A}.B + A.\bar{B}) + C_{in}.\overline{\bar{A}.B + A.\overline{B}} \quad \text{(4)}$$

Similarly, the expression for CARRY output can be rewritten as follows

$$C_{out} = B.C_{in}(A + \bar{A}) + A.B + A.C_{in}(B + \bar{B})$$

$$= A.B + A.B\,C_{in} + \bar{A}.B\,C_{in} + A.B\,C_{in} + A.\bar{B}\,C_{in}$$

$$= A.B + A.B\,C_{in} + \bar{A}.B\,C_{in} + A.\bar{B}\,C_{in}$$

$$= A.B(1 + C_{in}) + C_{in}(\bar{A}.B + A.\bar{B})$$

$$= A.B + C_{in}(\bar{A}.B + A.\bar{B}) \quad \text{(5)}$$

The full adder of the type described above forms the basic building block of binary adders. However, a single full adder circuit can be used to add one-bit binary numbers only.

A cascade arrangement of these adders can be used to construct adders capable of adding binary numbers with a larger number of bits. For example, a four-bit binary adder would require four full adders of the type shown in Figure (11) to be connected in cascade

Figure(12)shows such an arrangement. (A_3 A_2 A_1 A_0) and (B_3 B_2 B_1 B_0) are the two binary numbers to be added, with A_0 and B_0 representing LSBs and A3 and B3 representing MSBs of the two numbers.

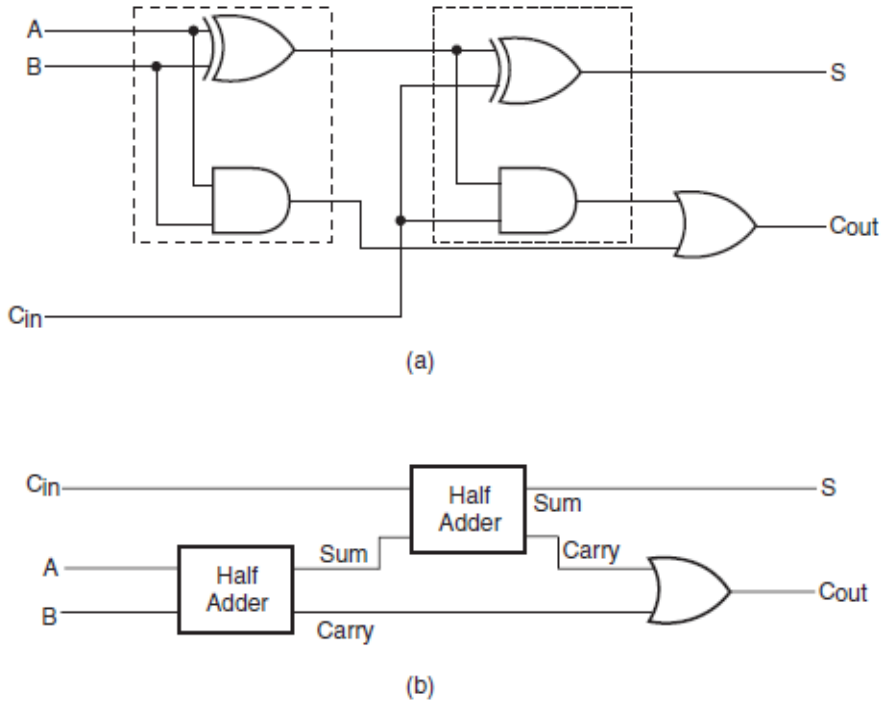


Figure 11 Logic implementation of a full adder with half – adders

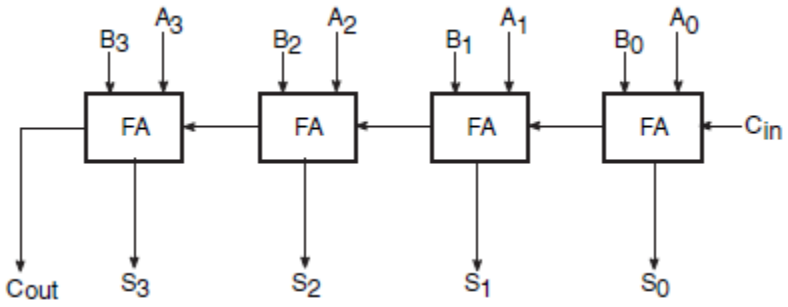


Figure 12 Four - bit binary adder

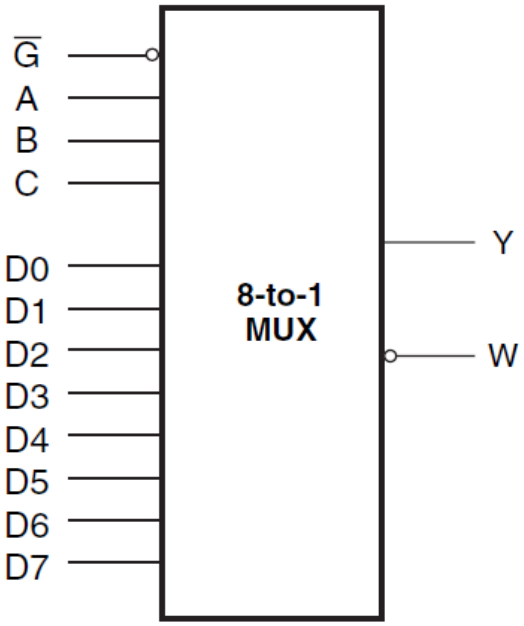
5.3.2Multiplexer(IC 74151):

A *multiplexer* or *MUX*, also called a *data selector*, is a combinational circuit with more than one input line, one output line and more than one selection line. There are some multiplexer ICs that provide complementary outputs.

Also, multiplexers in IC form almost invariably have an ENABLE or STROBE input, which needs to be active for the multiplexer to be able to perform its intended function. A

multiplexer selects binary information present on any one of the input lines, depending upon the logic status of the selection inputs, and routes it to the output line.

If there are n selection lines, then the number of maximum possible input lines is 2n and the multiplexer is referred to as a 2^n-to-1 multiplexer or $2^n \times 1$ multiplexer.



(a)

Inputs				Output	
Select			Enable		
C	B	A	$\overline{G}$	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

$\overline{G}$: ENABLE input
A, B, C : Select inputs
D0-D7 : Data inputs
Y,W : outputs

(b)

Figure 13 (a) 8 to 1 multiplier circuit representation (b) 8 to 1 multiplier truth table

5.3.3 Encoders:

An encoder is a multiplexer without its single output line. It is a combinational logic function that has 2^n (or fewer) input lines and n output lines, which correspond to n selection lines in a multiplexer.

The n output lines generate the binary code for the possible 2^n input lines. Let us take the case of an octal-to-binary encoder. Such an encoder would have eight input lines, each representing an octal digit, and three output lines representing the three-bit binary equivalent.

The truth table of such an encoder is given in Table. In the truth table, D_0 to D_7 represent octal digits 0 to 7. A, B and C represent the binary digits.

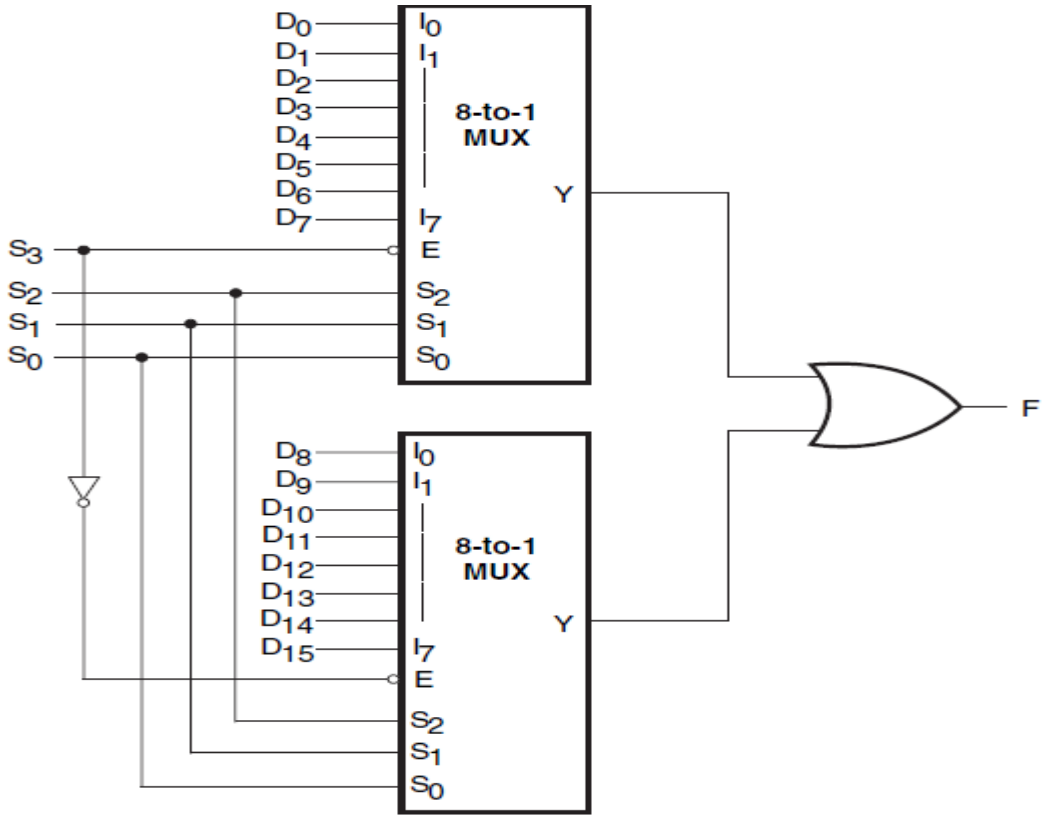


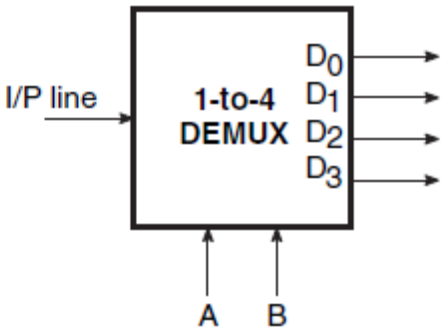
Figure 14

The eight input lines would have 2^8 = 256 possible combinations. However, in the case of an octal-to-binary encoder, only eight of these 256 combinations would have any meaning. The remaining combinations of input variables are 'don't care' input combinations. Also, only one of the input lines at a time is in logic '1' state.

5.3.4 Demultiplexers and Decoders:

A **demultiplexer** is a combinational logic circuit with an input line, 2^n output lines and n select lines. It routes the information present on the input line to any of the output lines. The output line that gets the information present on the input line is decided by the bit status of the selection lines.

A **decoder** is a special case of a demultiplexer without the input line. Figure 15(a) shows the circuit representation of a 1-to-4 demultiplexer. Figure 15(b) shows the truth table of the demultiplexer when the input line is held HIGH.



(a)

I/P	Select		O/P			
	A	B	D_0	D_1	D_2	D_3
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

(b)

Figure 15 1 - to - 4 demultipliers

A decoder is a combinational circuit that decodes the information on n input lines to a maximum of 2^n unique output lines can have a maximum of eight unique output lines.

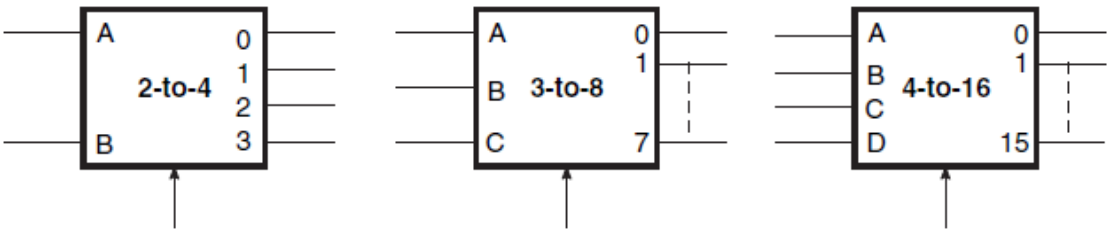


Figure 16 circuit representation of 2-to-4, 3-to8, 4-to-16 line decoders

Figure (16) shows the circuit representation of 2-to-4, 3-to-8 and 4-to-16 line decoders. If there are some unused or 'don't care' combinations in the n-bit code, then there will be fewer than 2n output lines. As an illustration, if there are three input lines, it can have a maximum of eight unique output lines. If, in the three-bit input code, the only used three-bit

combinations are 000, 001, 010, 100, 110 and 111 (011 and 101 being either unused or don't care combinations), then this decoder will have only six output lines.

In general, if n and m are respectively the numbers of input and output lines, then $m \leq 2^n$. A decoder can generate a maximum of 2n possible minterms with an n-bit binary code.

5.3.5 BCD to 7-segmentdecoder:

Seven-segment displays [Figure 17 (a)] are very common and are found almost everywhere, from pocket calculators, digital clocks and electronic test equipment to petrol pumps. A single seven-segment display or a stack of such displays invariably meets our display requirement. There are both LED and LCD types of seven – segment display.

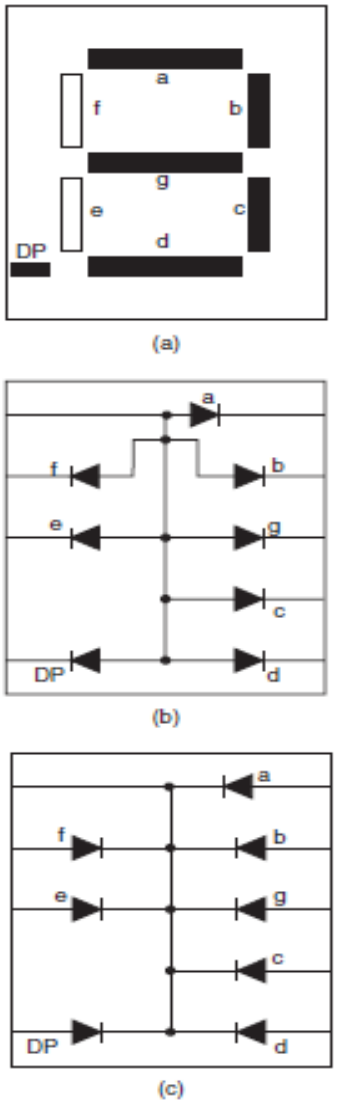


Figure 17 seven - segment displays

Common cathode type '1' means ON									Common anode type '0' means ON								
	a	b	c	d	e	f	g	DP		a	b	c	d	e	f	g	DP
0	1	1	1	1	1	1	0		0	0	0	0	0	0	0	1	
1	0	1	1	0	0	0	0		1	1	0	0	1	1	1	1	
2	1	1	0	1	1	0	1		2	0	0	1	0	0	1	0	
3	1	1	1	1	0	0	1		3	0	0	0	0	1	1	0	
4	0	1	1	0	0	1	1		4	1	0	0	1	1	0	0	
5	1	0	1	1	0	1	1		5	0	1	0	0	1	0	0	
6	0	0	1	1	1	1	1		6	1	1	0	0	0	0	0	
7	1	1	1	0	0	0	0		7	0	0	0	1	1	1	1	
8	1	1	1	1	1	1	1		8	0	0	0	0	0	0	0	
9	1	1	1	0	0	1	1		9	0	0	0	1	1	0	0	
a	1	1	1	1	1	0	1		a	0	0	0	0	0	1	0	
b	0	0	1	1	1	1	1		b	1	1	0	0	0	0	0	
c	0	0	0	1	1	0	1		c	1	1	1	0	0	1	0	
d	0	1	1	1	1	0	1		d	1	0	0	0	0	1	0	
e	1	1	0	1	1	1	1		e	0	0	1	0	0	0	0	
f	1	0	0	0	1	1	1		f	0	1	1	1	0	0	0	

Figure 18 seven - segment display code

There are common anode-type LED displays where the arrangement of different diodes, designated a, *b, c, d, e, f* and g, is as shown in Figure 17(b), and common cathode-type displays where the individual diodes are interconnected as shown in Figure 17 (c). Each display unit usually has a dot point (DP).

The DP could be located either towards the left (as shown) or towards the right of the figure '8' display pattern. This type of display can be used to display numerals from 0 to 9 and letters from A to F. figure 18 gives the binary code for displaying different numeric and alphabetic characters for both the common cathode and the common anode type displays. A '1' lights a segment in the common cathode type display, and a '0' lights a segment in the common anode type display.

5.4 SEQUENTIALCIRCUITSUSINGTTL74XXICs:

5.4.1 Flip Flops:

R-S Flip-Flop

A flip-flop is a bistable circuit. Both of its output states are stable. The circuit remains in a particular output state indefinitely until something is done to change that output status. Referring to the bistable multivibrator has two states were those of the output transistor in saturation (representing a LOW output) and in cut-off (representing a HIGH output). If the LOW

and HIGH outputs are respectively regarded as '0' and '1', then the output can either be a '0' or a '1'.

Since either a '0' or a '1' can be held indefinitely until the circuit is appropriately triggered to go to the other state, the circuit is said to have memory. It is capable of storing one binary digit or one bit of digital information.

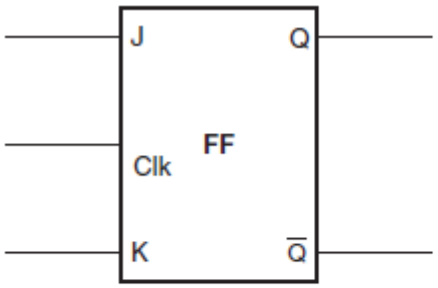
when one of the transistors was in saturation, the other was in cut-off. This implies that, if we had taken outputs from the collectors of both transistors, then the two outputs would be complementary.

In the flip-flops of various types that are available in IC form, these devices offer complementary outputs usually designated as Q and $\bar{Q}$ The R-S flip-flop is the most basic of all flip-flops. The letters 'R' and 'S' here stand for RESET and SET. When the flip-flop is SET, its Q output goes to a '1' state, and when it is RESET it goes to a '0' state. The Q output is the complement of the Q output at all times.

_J-K_ Flip-Flop

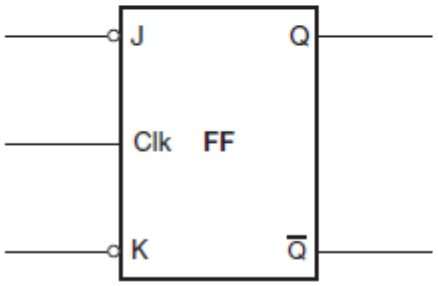
A J-K flip-flop behaves in the same fashion as an R-S flip-flop except for one of the entries in the function table. In the case of an R-S flip-flop, the input combination S = R = 1 (in the case of a flip-flop with active HIGH inputs) and the input combination S = R = 0 (in the case of a flip-flop with active LOW inputs) are prohibited.

In the case of a J-K flip-flop with active HIGH inputs, the output of the flip-flop toggles, that is, it goes to the other state, for J = K = 1 . The output toggles for J = K = 0 in the case of the flip-flop having active LOW inputs. Thus, a J-K flip-flop overcomes the problem of a forbidden input combination of the R-S flip-flop. Figures 17 (a) and (b) respectively show the circuit symbol of level-triggered J-K flip-flops with active HIGH and active LOW inputs, along with their function tables. Figure 18 shows the realization of a J-K flip-flop with an R-S flip-flop. The characteristic tables for a J-K flip-flop with active HIGH J and K inputs and a J-K flip-flop with active LOW J and K inputs are respectively shown in Figure 9 (a) and (b)_ The corresponding Karnaugh maps are shown in Figure 9 (c) for the characteristics table of Figure 9 (a) and in Fig. 9 (d) for the characteristic table of Figure 9 (b). The characteristic equations for the Karnaugh maps of Figure 9 (c) and (d) are respectively.



Operation Mode	J	K	Clk	Q_{n+1}
SET	1	0	1	1
RESET	0	1	1	0
NO CHANGE	0	0	1	Q_n
TOGGLE	1	1	1	$\overline{Q}_n$

(a)



Operation Mode	J	K	Clk	Q_{n+1}
SET	0	1	1	1
RESET	1	0	1	0
NO CHANGE	1	1	1	Q_n
TOGGLE	0	0	1	$\overline{Q}_n$

(b)

Figure 19

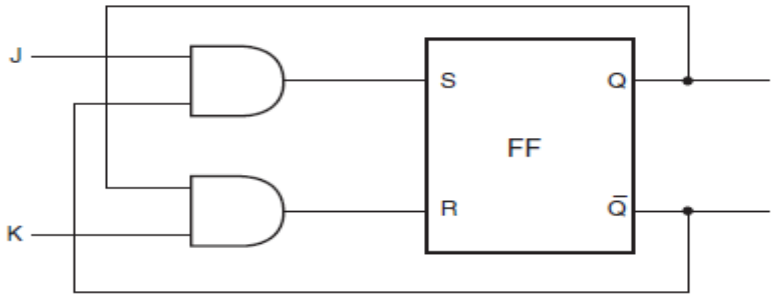


Figure 20

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

(a)

Q_n	J	K	Q_{n+1}
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

(b)

Q_n \ JK	00	01	11	10
0			1	1
1	1			1

(c)

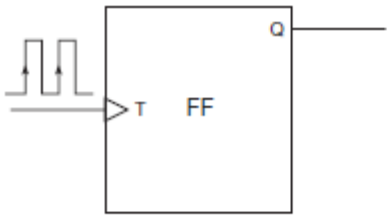
Q_n \ JK	00	01	11	10
0	1	1		
1		1	1	

(d)

Figure 21

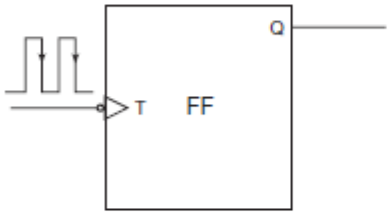
Toggle Flip-Flop (*T* Flip-Flop):

The output of a toggle flip-flop, also called a T flip-flop, changes state every time it is triggered at its T input, called the toggle input. That is, the output becomes '1' if it was '0' and '0' if it was '1'. Figures 20 (a) and (b) respectively show the circuit symbols of positive edge-triggered and negative edge-triggered T flip-flops, along with their function tables.



T	Q_n	Q_{n+1}
↑	0	1
↑	1	0

(a)



T	Q_n	Q_{n+1}
↓	0	1
↓	1	0

(b)

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

(c)

Q_n	T	Q_{n+1}
0	0	1
0	1	0
1	0	0
1	1	1

(d)

Figure 22 (a) positive edge-triggered toggle flip-flop (b) a megatove edge-triggered toggle flip-flop, (c,d) charcteristic tables of level-trigered toggle flip-flops and (e,f karnaugh maps for characteristic tables(c,d))

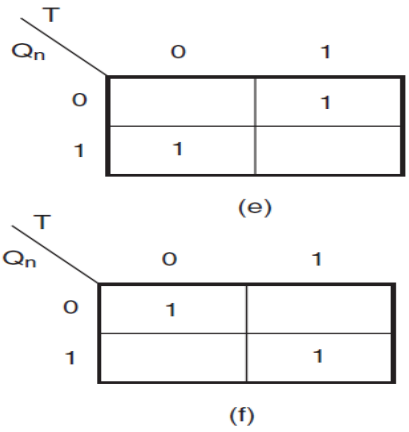


Figure 23 continued

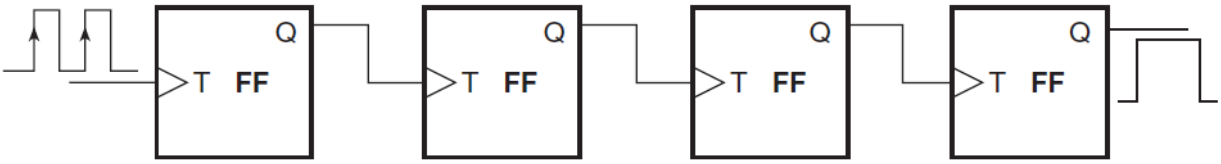


Figure 24 casecade arrangement of T flip-flops

Figures 21(a) and (b) respectively show the circuit symbols of positive edge-triggered and negative edge-triggered T flip flops, along with their function tables.

If we consider the T input as active when HIGH, the characteristic table of such a flip-flop is shown in Figure 21 (c). If the T input were active when LOW, then the characteristic table would be as shown in Figure 21 (d). The Karnaugh maps for the characteristic tables of Figure 21(c) and (d) are shown in Figure 21 (e) and (f) respectively. The characteristic equations as written from the Karnaugh maps are as follows:

$$Q_{n+1} = T.\bar{Q}_n + \bar{T}.Q_n$$

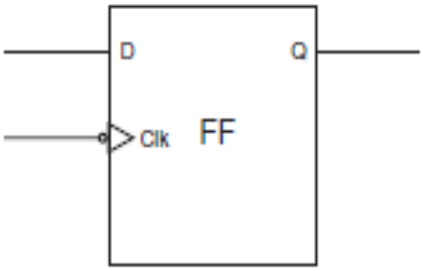
$$Q_{n+1} = \bar{T}.\bar{Q}_n + T.Q_n$$

It is obvious from the operational principle of the T flip-flop that the frequency of the signal at the Q output is half the frequency of the signal applied at the T input. A cascaded arrangement of nT flip-flops, where the output of one flip-flop is connected to the T input of the following flip-flop, can be used to divide the input signal frequency by a factor of 2^n. Figure 22 shows a divide-by-16 circuit built around a cascaded arrangement of four T flip-flops.

D Flip-Flop

A D flip-flop, also called a *delay flip-flop*, can be used to provide temporary storage of one bit of information. Figure 23 (a) shows the circuit symbol and function table of a negative edge-triggered D flip-flop.

When the clock is active, the data bit (0 or 1) present at the D input is transferred to the output. In the D flip-flop of Figure 23, the data transfer from D input to Q output occurs on the negative-going (HIGH-to-LOW) transition of the clock input. The D input can acquire new status when the clock is inactive, which is the time period between successive HIGH-to-LOW transitions. The D flip-flop can provide a maximum delay of one clock period.



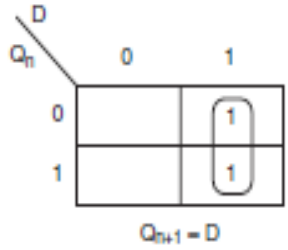
(a)

D	Clk	Q
0	↓	0
1	↓	1

(b)

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

(c)



(d)

Figure 25 D flip-flop

The characteristic table and the corresponding Karnaugh map for the D flip-flop of Figure 23 (a) are shown in Figure 23 (c) and (d) respectively. The characteristic equation is as follows:

$$Q_{n+1} = D$$

5.4.2 Shift Register:

A *shift register* is a digital device used for storage and transfer of data. The data to be stored could be the data appearing at the output of an encoding matrix before they are fed to the main digital system for processing or they might be the data present at the output of a microprocessor before they are fed to the driver circuitry of the output devices.

The shift register thus forms an important link between the main digital system and the input/output channels. The shift registers can also be configured to construct some special types of counter that can be used to perform a number of arithmetic operations such as subtraction, multiplication, division, complementation, etc.

The basic building block in all shift registers is the flipflop, mainly a D-type flip-flop. Although in many of the commercial shift register ICs their internal circuit diagram might indicate the use of *R-S* flip-flops, a careful examination will reveal that these *R-S* flip-flops have been wired as D flip-flops only.

The storage capacity of a shift register equals the total number of bits of digital data it can store, which in turn depends upon the number of flip-flops used to construct the shift register.

Since each flip-flop can store one bit of data, the storage capacity of the shift register equals the number of flip-flops used. As an example, the internal architecture of an eight-bit shift register will have a cascade arrangement of eight flip-flops.

Based on the method used to load data onto and read data from shift registers, they are classified as serial-in serial-out (SISO) shift registers, serial-in parallel-out (SIPO) shift registers, parallel-in serial-out (PISO) shift registers and parallel-in parallel-out (PIPO) shift registers. Figure 24 shows a circuit representation of the above-mentioned four types of shift register.

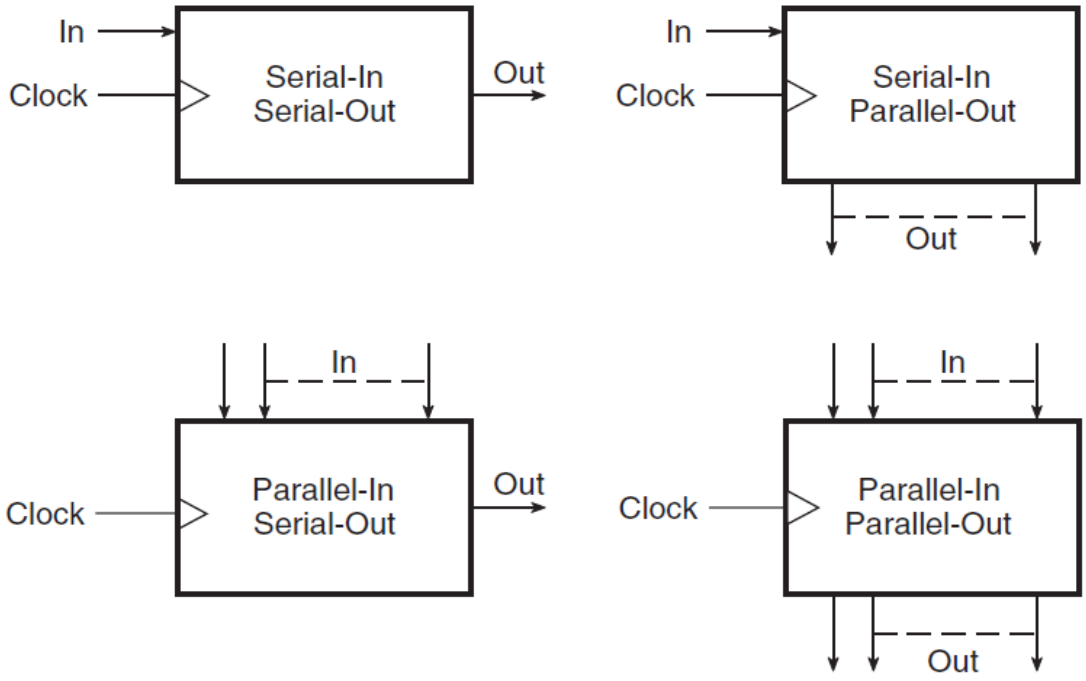
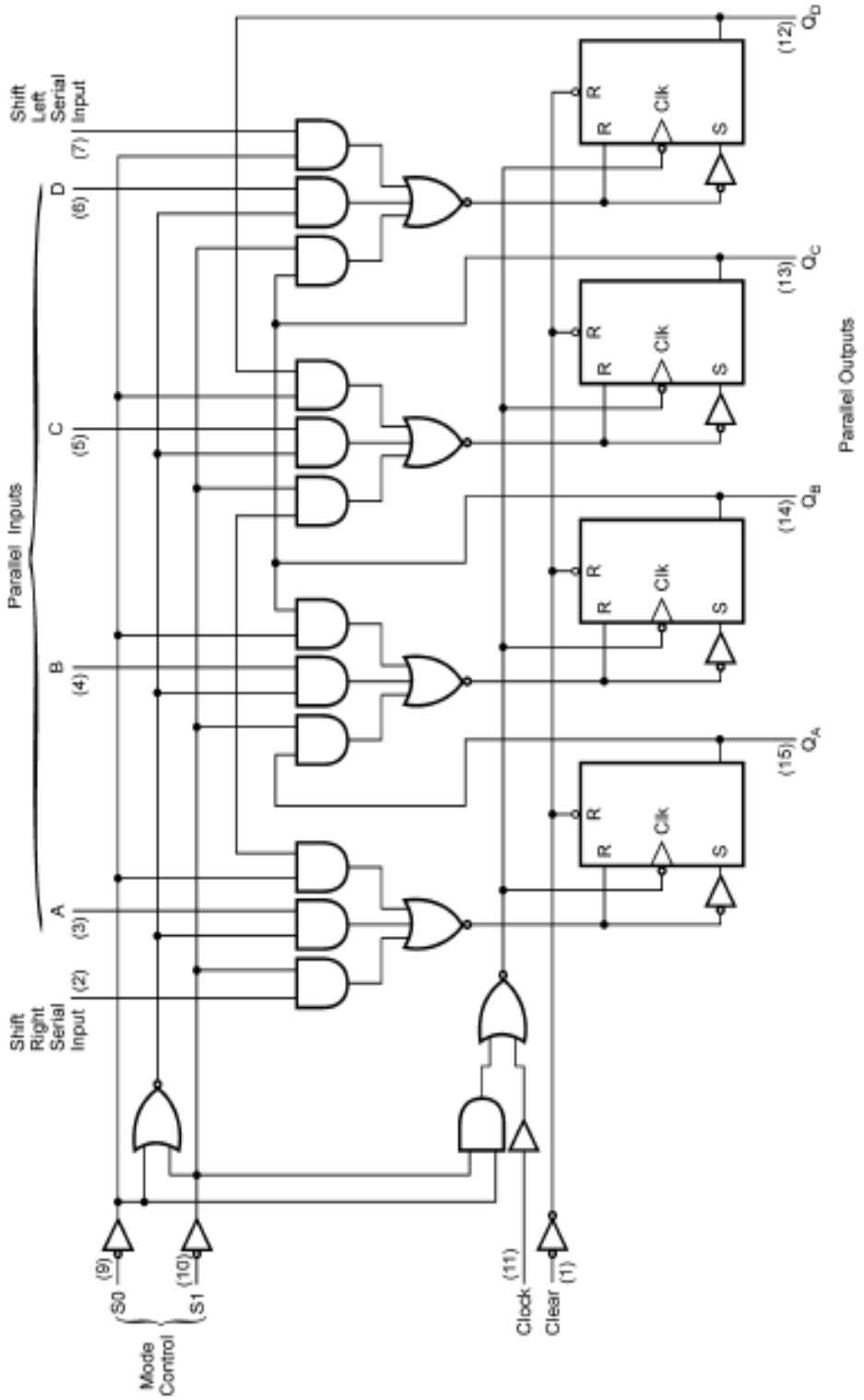


Figure 26 circuit representation of shift registers

5.4.3 Universal Shift Register(IC 74194):

A universal shift register can be made to function as any of the four types of register discussed in previous sections. That is, it has serial/parallel data input and output capability, which means that it can function as serial-in serial-out, serial-in parallel-out, parallel-in serial out and parallel-in parallel-out shift registers.

IC 74194 is a common four-bit bidirectional universal shift register. Figure 25 shows the logic diagram of Ic 74194. the device offers four modes of operation, namely (a) inhibit clock, (b) shift right, (c) shift left and (d) parallel load. Clocking of the device is inhibited when both the mode control inputs S_1 and S_0 are in the logic LOW state. shift right and shift left operations are accomplished synchronously with LOW-to-HIGH transition of the clock with S_1 LOW and S_0 HIGH (for shift right) and S_1 HIGH and S_0 LOW (for shift left).


Shift Left Serial Input
(7)
D
(6)
C
(5)
B
(4)
A
(3)
Shift Right Serial Input
(2)
Parallel Inputs
(9)
S0
(10)
S1
Mode Control
(11)
Clock
(1)
Clear
R
Clk
S
(12)
Q_D
(13)
Q_C
(14)
Q_B
(15)
Q_A
Parallel Outputs

Serial data are entered in the case of shift right and shift left operations at the corresponding data input terminals. Parallel loading is also accomplished synchronously with LOW-to-HIGH clock transitions by applying four bits of data and then driving the mode control inputs S1 and S0 to the logic HIGH state.

Data are loaded into corresponding flipflops and appear at the outputs with LOW-to-HIGH clock transition. Serial data flow is inhibited during parallel loading. Different modes of operation are apparent in the timing waveforms of Figure 26.

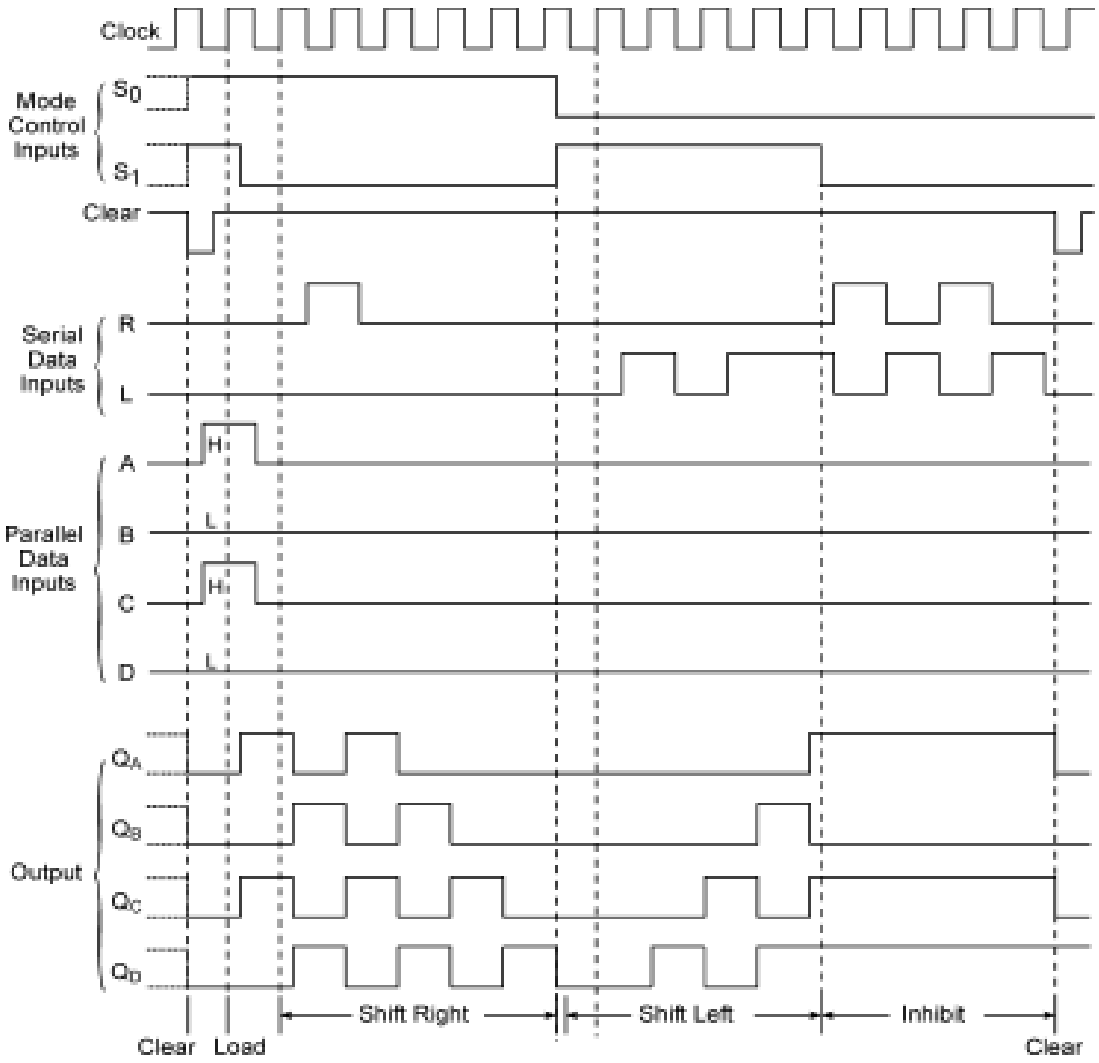


Figure 27 timing waveforms of IC 74194

5.4.3 Asynchronous binary counter:

A *ripple counter* is a cascaded arrangement of flip-flops where the output of one flip-flop drives the clock input of the following flip-flop. The number of flip-flops in the cascaded arrangement depends upon the number of different logic states that it goes through before it repeats the sequence, a parameter known as the modulus of the counter.

In a ripple counter, also called an *asynchronous counter* or a *serial counter*, the clock input is applied only to the first flip-flop, also called the input flip-flop, in the cascaded arrangement. The clock input to any subsequent flip-flop comes from the output of its immediately preceding flip-flop. For instance, the output of the first flip-flop acts as the clock input to the second flip-flop, the output of the second flip-flop feeds the clock input of the third flip-flop and so on. In general, in an arrangement of n flip-flops, the clock input to the nth flip-flop comes from the output of the $(n-1)^{th}$ flip-flop for n>1. Figure 27 shows the generalized block schematic arrangement of an n-bit binary ripple counter.

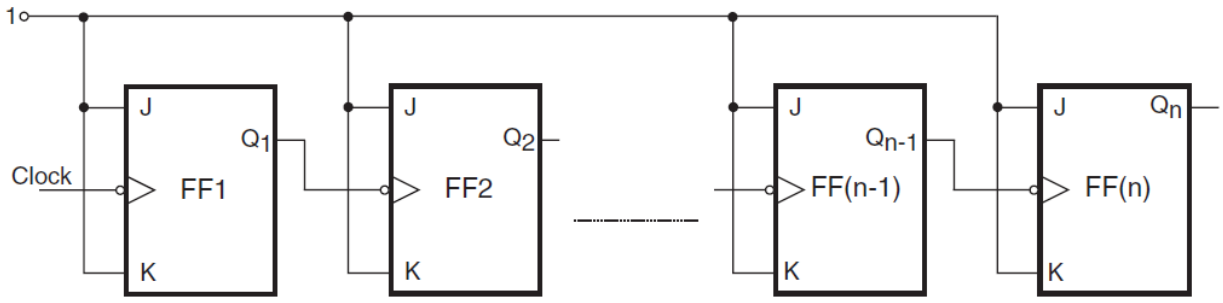


Figure 28 generalized block schematic of n-bit binary ripple counter

As a natural consequence of this, not all flip-flops change state at the same time. The second flip-flop can change state only after the output of the first flip-flop has changed its state. That is, the second flip-flop would change state a certain time delay after the occurrence of the input clock pulse owing to the fact that it gets its own clock input from the output of the first flip-flop and not from the input clock.

This time delay here equals the sum of propagation delays of two flip-flops, the first and the second flip-flops. In general, the nth flip-flop will change state only after a delay equal to n times the propagation delay of one flip-flop.

The term ‘ripple counter’ comes from the mode in which the clock information ripples through the counter. It is also called an ‘asynchronous counter’ as different flip-flops comprising the counter do not change state in synchronization with the input clock.

In a counter like this, after the occurrence of each clock input pulse, the counter has to wait for a time period equal to the sum of propagation delays of all flip-flops before the next clock pulse can be applied. The propagation delay of each flip-flop, of course, will depend upon the logic family to which it belongs.